XRT94L43FAQ

Frequently Asked Questions regarding the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/STM-4 Mapper IC

Preliminary

August 15, 2006

FREQUENTLY ASKED QUESTIONS REGARDING THE 12-CHANNEL DS3/E3/STS-1 TO STS-12/STM-4 MAPPER IC

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Q1: On-Chip Jitter Attenuator-related Questions.

Q1.1: What is APS Recovery Time of the XRT94L43 device?

A1.1: In all cases, the APS Recovery Time (of the XRT94L43 device) was measured to be less than 2ms (which is well within the 50ms APS Completion Time requirements, per Section 5.3.3.3 of Telcordia GR-253-CORE).

NOTE: If the user wishes to obtain more information on our approach to measuring the APS Recovery Time of the XRT94L43 device, then he/she should refer to "Test Report – Automatic Protection Switching (APS) Recovery Time Testing with the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12 Mapper IC – Revision C Silicon"

Q1.2: What Frequency Accuracy is required at the REFCLK34 (pin P23), REFCLK45 (pin P25) or REFCLK51 (pin P24) input pins?

A1.2: These input pins are used as a "Reference Clock" by the "Jitter Attenuator/Clock Smoother" PLLs within the De-Map Direction. The user is advised to apply a 34.368MHz ± 20ppm signal to the REFCLK34 input pin, a 44.736MHz ± 20ppm signal to the REFCLK45 input pin or a 51.84MHz ± 20ppm signal to the REFCLK51 input pin. This recommendation (of using clock signals with an accuracy of ±20ppm) is made in order to reduce or minimize the "LOCK" time of the "Clock Smoother PLL" within the XRT94L43 IC.

However, for minimal performance, the Clock Smoother PLL requires that the user supply a line-rate clock ± 750ppm. However, the use of a more accurate clock signal (at each of these pins) will improve chip performance (e.g., reduce the "LOCK" time).

Q1.3: If one only intends to support DS3 and STS-1/STM-0 signals via the XRT94L43 device, is it still necessary to supply a 34.368MHz clock signal to the REFCLK34 input pin?

A1.3: No, in this case the user should simply tie the REFCLK34 input pin to GND. In addition to tying the REFCLK34 input pin to GND, the user should also write the value "[1, 1]" into Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register-Byte 0" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	1	1	0	0	0	0	0

This setting will configure the Jitter Attenuators within the XRT94L43 device to handle DS3 and STS-1 signals.

The user will still need to supply a 44.736MHz ±20ppm signal to the REFCLK45 input pin; if he/she wishes to map and de-map DS3 signals into/from an STS-12/STM-4 signal. Likewise, the user will also still need to supply a 51.84MHz ± 20ppm signal to the REFCLK51 input pin; if he/she wishes to map and de-map STS-1/STM-0 signals into/from an STS-12/STM-4 signal.

Q1.4: If one only intends to support DS3 and E3 signals via the XRT94L43 device, is it still necessary to supply a 51.84MHz clock signal to the REFCLK51 input pin?

A1.4: No, in this case, the user should simply tie the REFCLK51 input pin to GND. IN addition to tying the REFCLK51 input pin to GND, the user should also write the value "[0, X]" into Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register – Byte 0" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	X	0	0	0	0	0

This setting will configure the Jitter Attenuators within the XRT94L43 device to handle DS3 and E3 signals.

The user will still need to supply a 44.736MHz ±20ppm signal to the REFCLK45 input pin; if he/she wishes to map and de-map DS3 signals into/from an STS-12/STM-4 signal. Likewise, the user will also still need to supply a 34.368MHz ±20ppm signal to the REFCLK34 input pin; if he/she wishes to map and de-map E3 signals into/from an STM-4 signal.

Q1.5: Are the DS3 signals, which are extracted out of the XRT94L43 device (from SONET) capable of complying with the Category 1 Intrinsic Jitter Requirements per Telcordia GR-253-CORE and ANSI T1.105.03-1994?

A1.5: Yes, each of the 12 channels, within the XRT94L43 device, contains a DS3/E3 Jitter Attenuator block, which operates in the "De-Map" direction. These Jitter Attenuator blocks actually consists of a very narrow-band PLL and a FIFO. The results of extensive testing (per Section 5.6 within Telcordia GR-253-CORE) indicate that each of these 12 channels complies with these Intrinsic Jitter Requirements.

NOTE: A detailed write up on how well the XRT94L43 complies with these Intrinsic Jitter Requirements, can be found in the report entitled "Test Report: Telcordia GR-253-CORE Category 1 Intrinsic Jitter Requirements (for DS3 Applications) Test Results for the XRT94L43 device (Revision C Silicon)".

Q1.6: What does one need to do in order to configure the XRT94L43 Device to support "Daisy-Chain" Testing?

A1.6: First of all, the basic concept behind Daisy-Chain Testing is that one can "snake" a given DS3 or E3 signal through each of the 12-channels (in a Daisy-Chain Manner). This "DS3" or "E3" signal could either by applied directly to one of the Ingress Direction Ports of the chip (via Test Equipment) or it could be applied to the XRT94L43 device via the Receive STS-12/STM-4 Port" (of the chip).

If the user wishes to configure the XRT94L43 device to support "Daisy-Chain" operation, then he/she needs to set the "on-chip" Jitter Attenuators to the correct bandwidth (for this operation). The user can accomplish this by setting the "Jitter Attenuator BW[2:0]" bit-fields (Bits 7 through 5, within the "Mode Control Register – Byte 1) to either [0, 1, 1] or [1, 0, 0] as depicted below.

Mode Control Register – Byte 1 (Indirect = 0x00, 0x1A, Direct Address = 0x011A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Jitter Attenuator BW[2:0]			Unused			STS-1 Access SEL[1:0]	
R/W	R/W	R/W	R/O	R/O	R/O	R/W	R/W
0 1	1 0	1 0	0	0	0	0	0

NOTES:

1. Setting Jitter Attenuator BW[2:0] to "[0, 1, 1]" configures the Jitter Attenuator Bandwidth to be 3.15Hz.
2. Setting Jitter Attenuator BW[2:0] to "[1, 0, 0]" configures the Jitter Attenuator Bandwidth to be 11.8Hz.
3. This setting applies to all 12 Jitter Attenuator blocks within the chip.
4. For normal applications (e.g., in which the customer is required to comply with either the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) or the Intrinsic Jitter requirements (per ITU-T G.783), then we recommend that the user set these bit-fields to "[0, 0, 0]".

Q2: Clock Synthesizer Block-Related Questions.

Q2.1: What Frequency Accuracy is required at the REFCLK input pin (pin R1)?

A2.1: The "REFCLK" input pin functions as a clock source for the on-chip 622.08MHz clock synthesizer block. The XRT94L43 device contains an on-chip clock synthesizer that can be configured to generate a 622.08MHz clock signal from either of the following clock frequencies.

- 77.76MHz
- 51.84MHz
- 19.44MHz
- 12.96MHz

NOTES:

1. In many SONET/SDH systems, the user is required to operate with a line-rate ± 4.6ppm clock signal. If the user is required to generate and transmit data at a rate of 622.08MHz ± 4.6ppm, then the user will need to make sure that the above-mentioned clock source signals (which are supplied to the REFCLK input pin) are of equal frequency accuracy (±4.6ppm).
2. Similarly, if the user is only required to generate and transmit data at a rate of 622.08MHz ± 20ppm, then the user will need to make sure that the above-mentioned clock source signals (which are supplied to the REFCLK input pin) are of equal frequency accuracy (±20ppm).

Q2.2: How does one configure the Clock Synthesizer block to synthesize a 77.76MHz clock signal, when provided with a 19.44MHz clock signal?

A2.2: The user accomplishes this by (1) supplying a 19.44MHz clock signal to the "REFCLK" input pin, and then, (2) writing the value 0x60 into the "Interface Control Register – Byte 2" as depicted below.

Interface Control Register – Byte 2 (Indirect Address = 0x00, 0x31; Direct Address = 0x0131)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REFFREQ[1:0]		Synth Clock	Ext 622	Unused			
R/W	R/W	R/W	R/W	R/O	R/O	R/O	R/O
0	1	1	0	0	0	0	0

This setting configures the Clock Synthesizer block to externally accept a 19.44MHz clock signal via the REFCLK (pin R4) pin, and internally synthesize a 77.76MHz clock signal from this signal.

Q2.3 How does one configure the XRT94L43 Device to use the 77.76MHz clock signal (which is supplied to the REFCLK input pin) as a timing reference?

A2.3: The user accomplishes this by doing the following.

STEP 1 – Supply a 77.76MHz clock signal to the REFCLK input pin (pin R4).

STEP 2 – Write the value "0xC0" into the "Interface Control Register – Byte 2" as depicted below.

Interface Control Register – Byte 2 (Indirect Address = 0x00, 0x31; Direct Address = 0x0131)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REFFREQ[1:0]		Synth Clock	Ext 622	Unused			
R/W	R/W	R/W	R/W	R/O	R/O	R/O	R/O
1	1	0	0	0	0	0	0

In this configuration setting, the internal circuitry (within the XRT94L43 device) is being directly clocked by the 77.76MHz clock signal that is being provided to the REFCLK input pin. The Clock Synthesizer is "by-passed".

NOTE: If the user intends to transmit the outbound STS-12/STM-4 data via the "Transmit STS-12/STM-4 PECL Interface", then the user will need to enable the clock synthesizer block by also setting Bit 5 (Synth Clock) within the "Interface Control Register – Byte 2" to "1" as depicted below.

Interface Control Register – Byte 2 (Indirect Address = 0x00, 0x31; Direct Address = 0x0131)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REFFREQ[1:0]		Synth Clock	Ext 622	Unused			
R/W	R/W	R/W	R/W	R/O	R/O	R/O	R/O
1	1	1	0	0	0	0	0

The user MUST enable the Clock Synthesizer block in order to internally synthesize the 622.08MHz clock necessary for the Transmit STS-12/STM-4 PECL Interface to operate.

Q3: General Configuration-Related Questions.

Q3.1 Is it permissible to configure the XRT94L43 device to support combinations of the STS-3 Telecom Bus Interface and the DS3/E3/STS-1 Interface?

A3.1: Yes, the XRT94L43 device can be thought of as consisting of 4 "STS-3 Blocks". Each of these "STS-3 Blocks" can be configured to function as either an STS-3 Telecom Bus interface or 3 DS3/E3/STS-1 interfaces. Each of these four (4) "STS-3 Blocks" can be configured independent of each other.

The user can configure a given "STS-3 Block" to operate in either the "STS-3 Telecom Bus" or in the DS3/E3/STS-1 Mode by writing the appropriate value into Bit 7 (STS-3 # N TB ON), within each of the following registers.

- Interface Control Register – Byte 3 – STS-3 Telecom Bus 3 (Indirect Address = 0x00, 0x38; Direct Address = 0x0138)
- Interface Control Register – Byte 2 – STS-3 Telecom Bus 2 (Indirect Address = 0x00, 0x39; Direct Address = 0x0139)
- Interface Control Register – Byte 1 – STS-3 Telecom Bus 1 (Indirect Address = 0x00, 0x3A; Direct Address = 0x013A)
- Interface Control Register – Byte 0 – STS-3 Telecom Bus 0 (Indirect Address = 0x00, 0x3B; Direct Address = 0x013B)

The bit-format of each of these registers is identical, and is presented below for completeness.

Interface Control Register – Byte N – STS-3 Telecom Bus 3 (Indirect Address = 0x00, 0x38 – 0x3B; Direct Address = 0x0138 – 0x013B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # N ON	TB BUS Disable	Unused	STS TB Parity Type	STS-3 TB J1 ONLY	STS-3 TB Parity Odd	STS-3 TB Parity Enable	STS-3 Rephase
R/W	R/W	R/0	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X

Setting Bit 7 (STS-3 TB # N ON) to "1" configures "STS-3 Block" Number "N" to operate in the "STS-3 Telecom Bus" Mode. Conversely, setting this bit-field to "0" configures "STS-3 Block" Number "N" to operate in the DS3/E3/STS-1 Mode.

The Mapping between the DS3/E3/STS-1 Channels and the STS-3 Telecom Bus Interface Channels

As indicated in the text above, if the user enables a certain STS-3 Telecom Bus, then certain DS3/E3/STS-1 Channels will be disabled. The following table presents the relationship between each of the STS-3 Telecom Bus Interfaces and the corresponding DS3/E3/STS-1 Channels.

Table 3-1, The Mapping between the DS3/E3/STS-1 Channels and the STS-3 Telecom Bus Interface Channel

STS-3 Telecom Bus Interface Channel	Corresponding DS3/E3/STS-1 Channels
0	0, 4, 8
1	1, 5, 9
2	2, 6, 10
3	3, 7, 11

Q3.2 How does one configure a given channel to operate in the DS3/E3 Framer Mode?

The XRT94L43 device can be configured to operate in two basic modes.

- STS-3 to STS-12 Mapper Mode
- STS-1/DS3/E3 to STS-12/STM-4 Mapper Mode.

If one configures the XRT94L43 device to operate in the "STS-3 to STS-12 Mapper" Mode, then many input/output pins will be configured to function as "19.44MHz Telecom Bus Interface" pins. Conversely, if one configures the XRT94L43 device to operate in the "STS-1/DS3/E3 to STS-12/STM-4 Mapper" Mode, then many input/output pins will be configured to function as Clock and Data Interfaces to external DS3/E3/STS-1 LIU devices.

Unfortunately, these Telecom Bus pins and the "LIU Interface" pins are one in the same. Therefore, if the user wishes to operate the XRT94L43 device in the "STS-1/DS3/E3 to STS-12 Mapper" Mode, then he/she must disable the STS-3 Telecom Bus Interface blocks.

This is accomplished by executing the following four steps.

STEP 1 – Disable Telecom Bus # 3

This is accomplished by setting Bit 7 (STS-3 TB # 3 ON) to "0", as illustrated below.

Interface Control Register – Byte 3 – STS-3 Telecom Bus 3 (Indirect Address = 0x00, 0x38; Direct Address = 0x0138)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 3 ON	TB BUS DIS	Unused	STS TB PAR_TYP	STS3 TB J1 ONLY	STS-3 TB PAR ODD	STS3 TB PAR ENB	STS3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STEP 2 – Disable Telecom Bus # 2

This is accomplished by setting Bit 7 (STS-3 TB # 2 ON) to "0", as illustrated below.

Interface Control Register – Byte 2 – STS-3 Telecom Bus 2 (Indirect Address = 0x00, 0x39; Direct Address = 0x0139)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 2 ON	TB BUS DIS	Unused	STS TB PAR_TYP	STS3 TB J1 ONLY	STS3 TB PAR ODD	STS3 TB PAR ENB	STS3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STEP 3 – Disable Telecom Bus # 1

This is accomplished by setting Bit 7 (STS-3 TB # 1 ON) to "0", as illustrated below.

Interface Control Register – Byte 1 – STS-3 Telecom Bus 1 (Indirect Address = 0x00, 0x3A; Direct Address = 0x013A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 1 ON	TB BUS DIS	Unused	STS TB PAR_TYP	STS3 TB J1 ONLY	STS3 TB PAR ODD	STS3 TB PAR ENB	STS3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STEP 4 – Disable Telecom Bus # 0

This is accomplished by setting Bit 7 (STS-3 TB # 0 ON) to "0", as illustrated below.

Interface Control Register – Byte 0 – STS-3 Telecom Bus 0 (Indirect Address = 0x00, 0x3B; Direct Address = 0x013B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 0 ON	TB BUS DIS	Unused	STS3/12 TB PAR_TYP	STS3/12 TB J1 ONLY	STS3/12 TB PAR ODD	STS3/12 TB PAR ENB	STS3/12 REPHASE STS-3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

If the user executes each of these four (4) steps, then all of the STS-3 Telecom Bus pins will now be configured to function as "DS3/E3/STS-1 LIU Interface" pins.

STEP 5 - Configuring the DS3/E3/STS-1 Channel Blocks to support DS3/E3 Applications

If the user wishes to configure a given channel, to operate in the DS3/E3 Mode, then he/she can accomplish this by setting both Bits 1 (Receive STS-1 Enable) and 0 (Transmit STS-1 Enable), within the corresponding Mapper Control Registers (Byte 2) to "0" as illustrated below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 OH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Ingress STS-1 Enable	Egress STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTES:

a. Setting Bits 1 (Receive STS-1 Enable) and Bits 0 (Transmit STS-1 Enable) to "1" would configure the Channel to operate in the STS-1 Mode.

b. The Indirect Address Location of the "Mapper Control Register – Byte 2" is 0xN6, 0x01; where "N" denotes the channel number and can range from "1" to "C".

Q3.3 How does one configure a given channel to operate in the STS-1 Mode?

The XRT94L43 device can be configured to operate in two basic modes.

- STS-3 to STS-12 Mapper Mode
- STS-1/DS3/E3 to STS-12/STM-4 Mapper Mode.

If one configures the XRT94L43 device to operate in the "STS-3 to STS-12 Mapper" Mode, then many input/output pins will be configured to function as "19.44MHz Telecom Bus Interface" pins. Conversely, if one configures the XRT94L43 device to operate in the "STS-1/DS3/E3 to STS-12/STM-4 Mapper" Mode, then many input/output pins will be configured to function as Clock and Data Interfaces to external DS3/E3/STS-1 LIU devices.

Unfortunately, these Telecom Bus pins and the "LIU Interface" pins are one in the same. Therefore, if the user wishes to operate the XRT94L43 device in the "STS-1/DS3/E3 to STS-12 Mapper" Mode, then he/she must disable the STS-3 Telecom Bus Interface blocks.

This is accomplished by executing the following four steps.

STEP 1 – Disable Telecom Bus # 3

This is accomplished by setting Bit 7 (STS-3 TB # 3 ON) to "0", as illustrated below.

Interface Control Register – Byte 3 – STS-3 Telecom Bus 3 (Indirect Address = 0x00, 0x38; Direct Address = 0x0138)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 3 ON	TB BUS DIS	Unused	STS TB PAR_TYP	STS3 TB J1 ONLY	STS-3 TB PAR ODD	STS3 TB PAR ENB	STS3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STEP 2 – Disable Telecom Bus # 2

This is accomplished by setting Bit 7 (STS-3 TB # 2 ON) to "0", as illustrated below.

Interface Control Register – Byte 2 – STS-3 Telecom Bus 2 (Indirect Address = 0x00, 0x39; Direct Address = 0x0139)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 2 ON	TB BUS DIS	Unused	STS TB PAR_TYP	STS3 TB J1 ONLY	STS3 TB PAR ODD	STS3 TB PAR ENB	STS3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STEP 3 – Disable Telecom Bus # 1

This is accomplished by setting Bit 7 (STS-3 TB # 1 ON) to "0", as illustrated below.

Interface Control Register – Byte 1 – STS-3 Telecom Bus 1 (Indirect Address = 0x00, 0x3A; Direct Address = 0x013A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 1 ON	TB BUS DIS	Unused	STS TB PAR_TYP	STS3 TB J1 ONLY	STS3 TB PAR ODD	STS3 TB PAR ENB	STS3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STEP 4 – Disable Telecom Bus # 0

This is accomplished by setting Bit 7 (STS-3 TB # 0 ON) to "0", as illustrated below.

Interface Control Register – Byte 0 – STS-3 Telecom Bus 0 (Indirect Address = 0x00, 0x3B; Direct Address = 0x013B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 TB # 0 ON	TB BUS DIS	Unused	STS3/12 TB PAR_TYP	STS3/12 TB J1 ONLY	STS3/12 TB PAR ODD	STS3/12 TB PAR ENB	STS3/12 REPHASE STS-3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

If the user executes each of these four (4) steps, then all of the STS-3 Telecom Bus pins will now be configured to function as "DS3/E3/STS-1 LIU Interface" pins.

STEP 5 – Configure the Jitter Attenuator Block to handle STS-1 signals
Set Bits 6 and 5 (SDH JA Freq_Sel[1:0]) to the value "[1, X]", as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	1	X	0	0	0	0	0

This setting will configure the Jitter Attenuator blocks to be able to handle an STS-1 signal.

NOTE: For most North American Applications, the user may wish to write the value "[1, 1]" into these bit-fields. This will configure the Jitter Attenuator blocks to handle both STS-1 and DS3 signals.

STEP 6 - Configuring the DS3/E3/STS-1 Channel Blocks to support STS-1 Applications
If the user wishes to configure a given channel, to operate in the STS-1 Mode, then he/she can accomplish this by setting both Bits 1 (Receive STS-1 Enable) and 0 (Transmit STS-1 Enable), within the corresponding Mapper Control Registers (Byte 2) to "1" as illustrated below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 OH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Ingress STS-1 Enable	Egress STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

NOTES:
a. Setting Bits 1 (Receive STS-1 Enable) and 0 (Transmit STS-1 Enable) to "0" would configure the Channel to operate in the DS3/E3 Mode.
b. The Indirect Address Location of the "Mapper Control Register – Byte 2" is 0xN6, 0x01; where "N" denotes the channel number and can range from "1" to "C".

Q3.4: What type of Loop-back Modes are available within the XRT94L43 device?

A3.4The XRT94L43 device supports all of the following loop-back modes.

- The Remote Line Loop-back Mode
- The Local Transport Loop-back Mode
- The Local Path Loop-back Mode
- STS-1 Local Loop-back Mode
- STS-1 Remote Loop-back Mode
- DS3/E3 Framer Local Loop-back Mode
- DS3/E3 Framer Remote Loop-back Mode

An illustration and description of each of these Loop-back Modes are presented below.

Remote Line Loop-back Mode

In this mode, all data, which is received by the "Receive STS-12/STM-4 PECL Interface" block will be routed to the "Transmit STS-12/STM-4 PECL Interface" block, as depicted below.

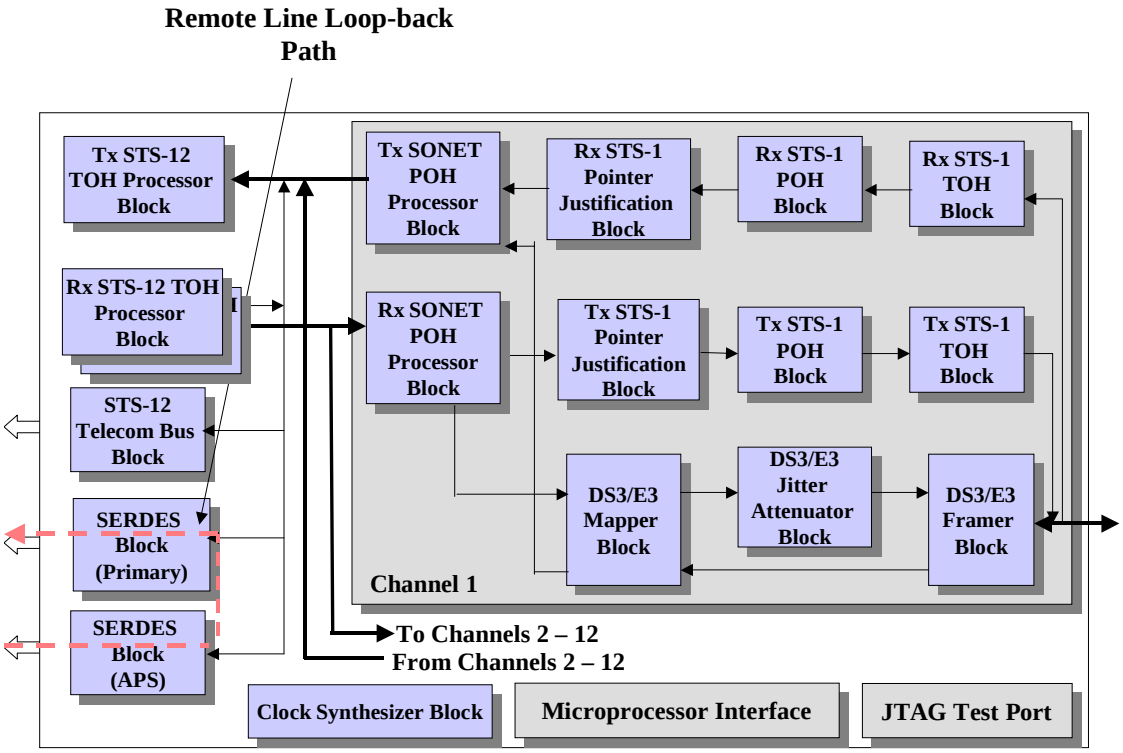

Figure 3-1, Illustration of the Remote Line Loop-back Mode

NOTE: In the Remote Line Loop-back Mode, the STS-12/STM-4 signal is not routed through any XRT94L43 Framer block circuitry.

Local Transport Loop-back Mode

In this mode, all data, which is being output via the "Transmit STS-12 TOH Processor" block, will be internally routed to the "Receive STS-12 TOH Processor" block as depicted below.

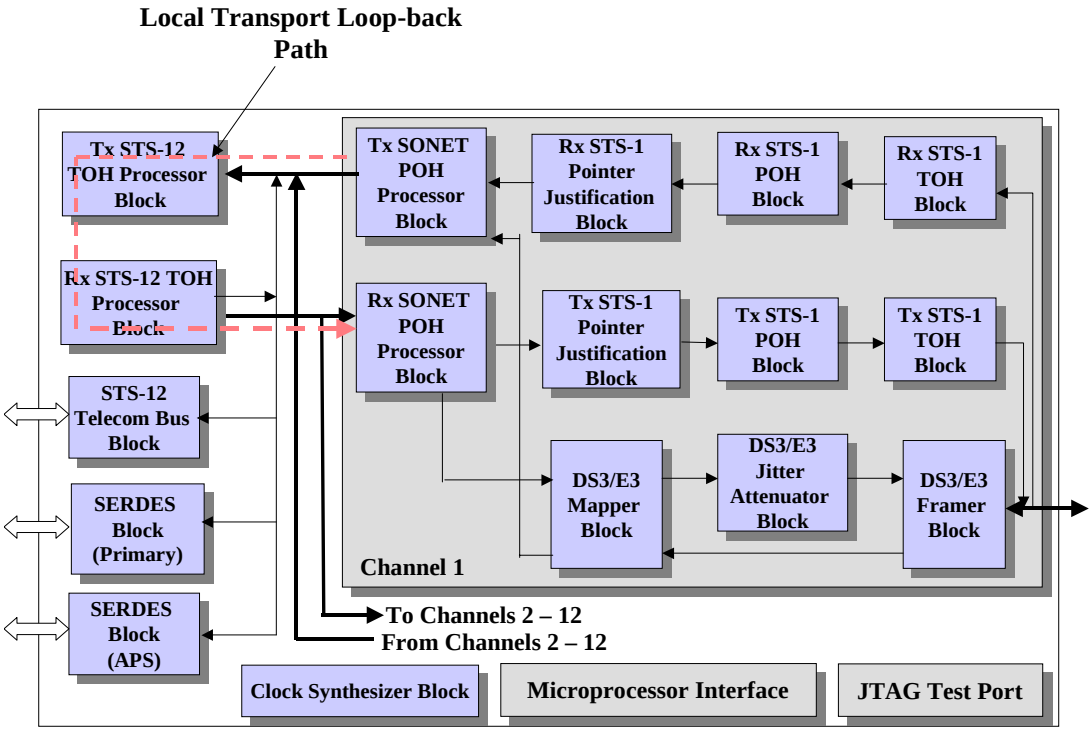

Figure 3-2, Illustration of the Local Transport Loop-back Mode

NOTE: If the user configures the XRT94L43 device to operate in the "Local Transport Loop-back" Mode, then, in addition to "routing" the "Transmit Output STS-12 data back into the "Receive Path (as depicted in Figure 3-2), the Transmit Output STS-12 data is still output via either the "Transmit STS-12/STM-4 PECL Interface" or the "Transmit STS-12/STM-4 Telecom Bus Interface", depending upon user configuration.

Local Path Loop-back Mode
In this mode, all data, which is being transmitted by the Transmit SONET POH Processor block will be internally routed back into the receive input of the Receive SONET POH Processor block.

NOTE: If the user invokes the "Local Path Loop-back" Mode, then this loop-back path will exist for all 12 channels, within the XRT94L43 device.

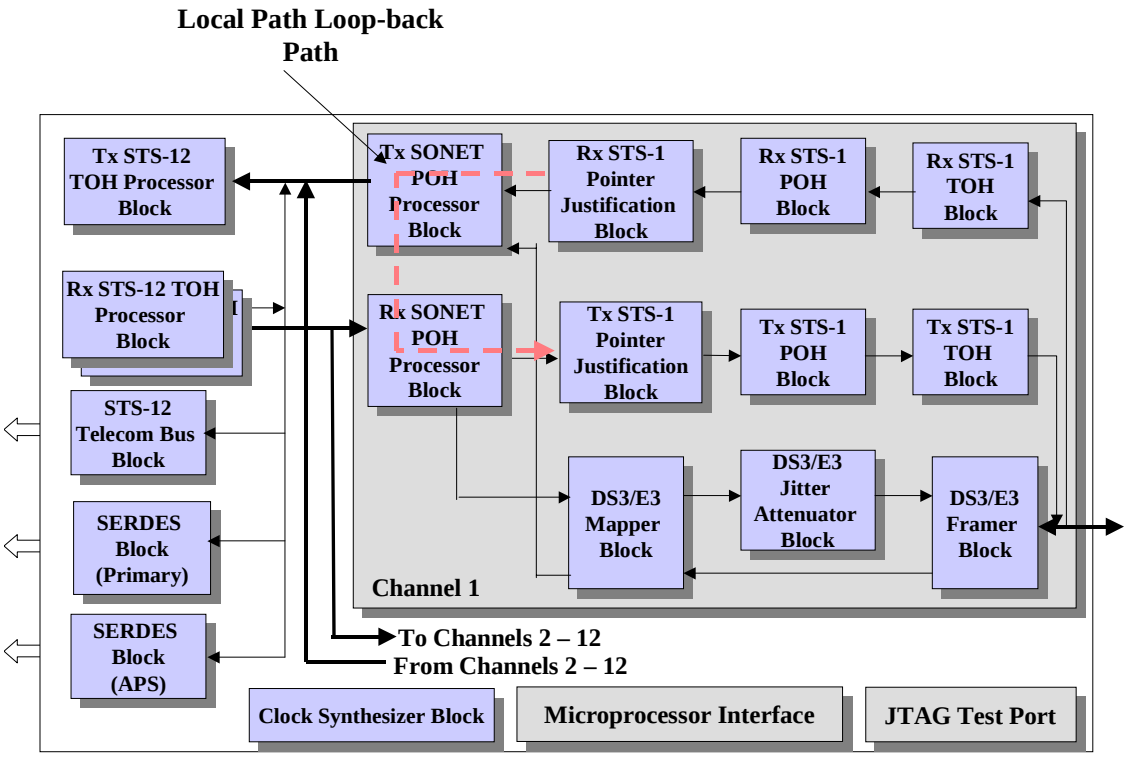

Figure 3-3, Illustration of the Local Path Loop-back Mode

STS-1 Local Loop-back Mode

In this mode, all data that is being output via the "Transmit STS-1 TOH Processor" block will be internally routed to the "Receive STS-1 TOH Processor" block, as depicted below.

NOTE: This loop-back mode can be configured on a "per-channel" basis.

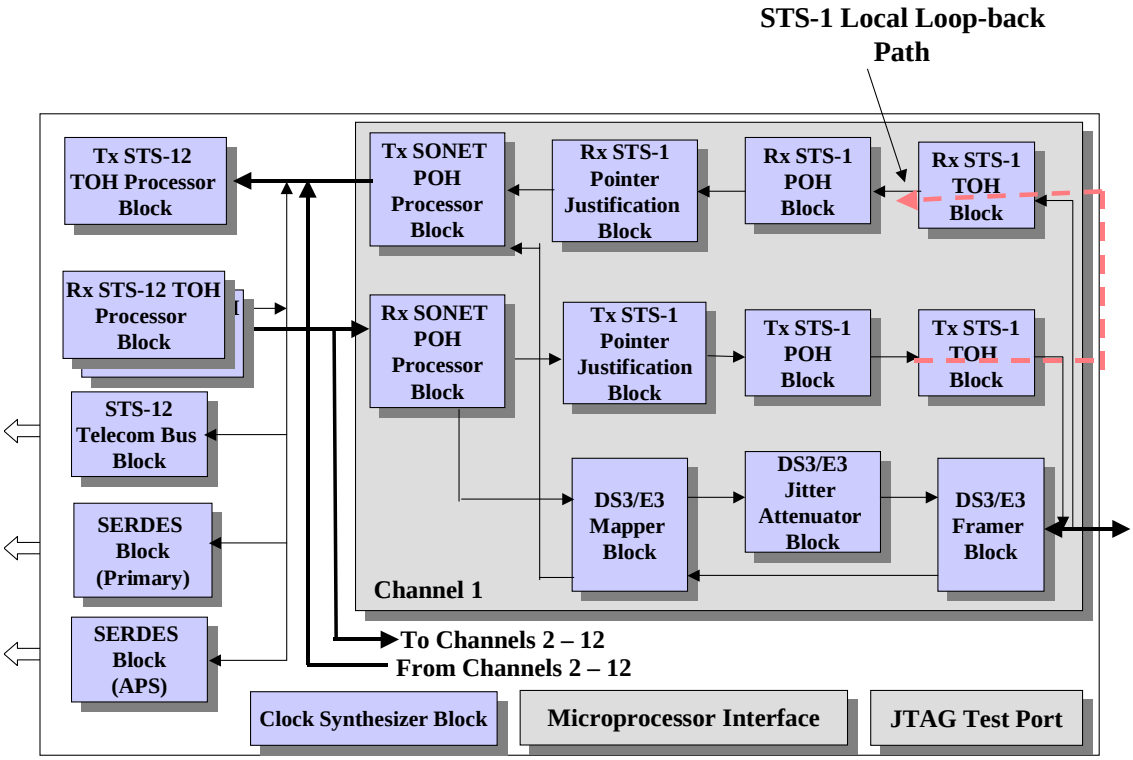

Figure 3-4, Illustration of the STS-1 Local Loop-back Mode

STS-1 Remote Loop-back Mode

In this mode, all data, which is received by a given channel (within the XRT94L43 device) at the Receive STS-1 Input will be internally routed to the Transmit STS-1 Output.

NOTES:

1. The STS-1 Remote Loop-back signal path is NOT routed through the Receive STS-1 TOH Processor and Transmit STS-1 TOH Processor blocks.
2. This loop-back mode can be configured on a "per-channel" basis.

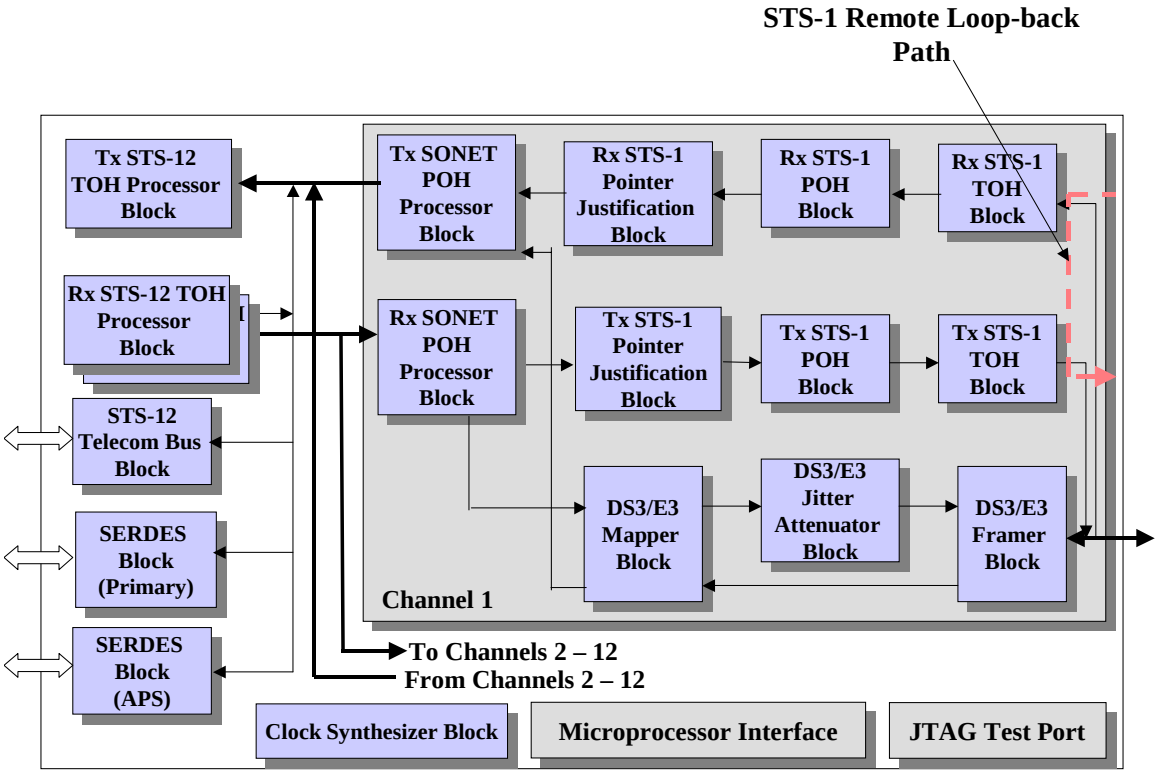

Figure 3-5, Illustration of the STS-1 Remote Loop-back Mode

Q3.5: How does one configure the XRT94L43 device to operate in the "Remote Line Loop-back" Mode?

A3.5: The user accomplishes this by writing the value "0x01" into the "Loop-back Control Register – Byte 0" as depicted below.

Loop-back Control Register – Byte 0 (Indirect Address = 0x00, 0x1F; Direct Address = 0x011F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				Loop-back[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

For completeness sake, an illustration of the XRT94L43 device, when configured to operate in the Remote Local Loop-back Mode is presented below in Figure 3-6.

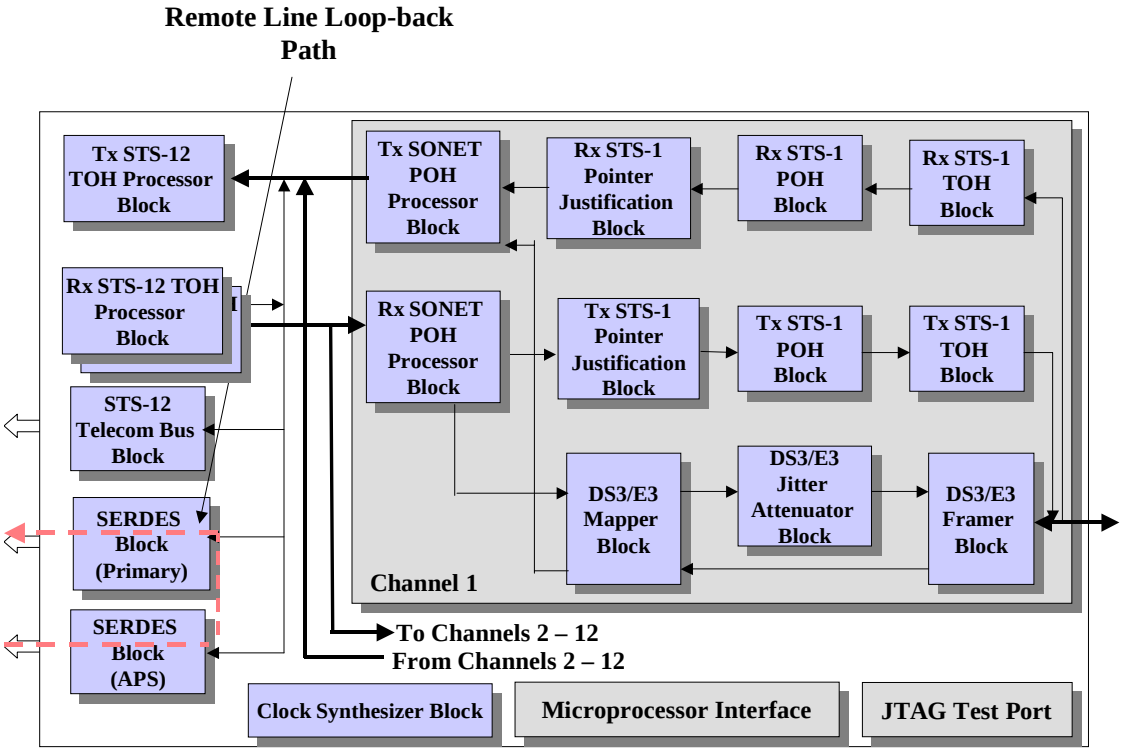

Figure 3-6, Illustration of the XRT94L43 Device, when configured to operate in the Remote Line Loop-back Mode

Q3.6: How does one configure the XRT94L43 device to operate in the "Local Transport Loop-back" Mode?

A3.6: The user accomplishes this by executing the following steps.

STEP 1: Disable the "Auto AIS-P Downstream upon the various STS-12 Defect conditions" feature.

The user can accomplish this by executing the following two sub-steps.

STEP 1a: Writing the value "0x00" into the "Receive STS-12 Transport – Auto AIS Control Register" as depicted below.

Receive STS-12 Transport – Auto AIS Control Register (Indirect Address = 0x04, 0x63; Direct Address = 0x0563)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit AIS-P (Down-stream) Upon J0 Message Unstable	Transmit AIS-P (Down-stream) Upon J0 Message Mismatch	Transmit AIS-P (Down-stream) Upon SF	Transmit AIS-P (Down-stream) Upon SD	Transmit AIS-P (Down-stream) upon Loss of Optical Carrier AIS	Transmit AIS-P (Down-stream) upon LOF	Transmit AIS-P (Down-stream) upon LOS	Transmit AIS-P (Down-stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: If the user executes this step, then he/she will prevent the Receive STS-12 TOH Processor block from automatically transmitting the AIS-P indicator, in the downstream direction (towards the twelve Receive SONET POH Processor blocks) should it (the Receive STS-12 TOH Processor block) declare any of the above-mentioned defect conditions while attempting to execute "Local-Transport" Loop-back.

STEP 1b: Writing the value "0x00" into the "Receive STS-12 Transport – Auto AIS (in Downstream STS-1s) Control Register, as depicted below.

Receive STS-12 Transport – Auto AIS (in Downstream STS-1s) Control Register (Indirect Address = 0x04, 0x6B; Direct Address = 0x056B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	Unused	Transmit AIS-P (via Downstream STS-1s) upon LOS	Transmit AIS-P (via Downstream STS-1s) upon LOF	Transmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	AIS-L Output Enable	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: If the user executes this step, then he/she will prevent each of the twelve (12) Transmit STS-1 TOH Processor block from automatically transmitting the AIS-P indicator, in the downstream direction (towards the DS3/E3/STS-1 LIU Devices) should the Receive STS-12 TOH Processor block declare any of the above-mentioned defect conditions while attempting to execute "Local-Transport" Loop-back.

STEP 2 – Configure the XRT94L43 device to operate in the Local-Transport Loop-back Mode.

The user accomplishes this by writing the value "0x02" into the "Loop-back Control Register – Byte 0" as depicted below.

Loop-back Control Register – Byte 0 (Indirect Address = 0x00, 0x1F; Direct Address = 0x011F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				Loop-back[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	0

For completeness sake, an illustration of the XRT94L43 device, when configured to operate in the Local Transport Loop-back Mode is presented below in Figure 3-7.

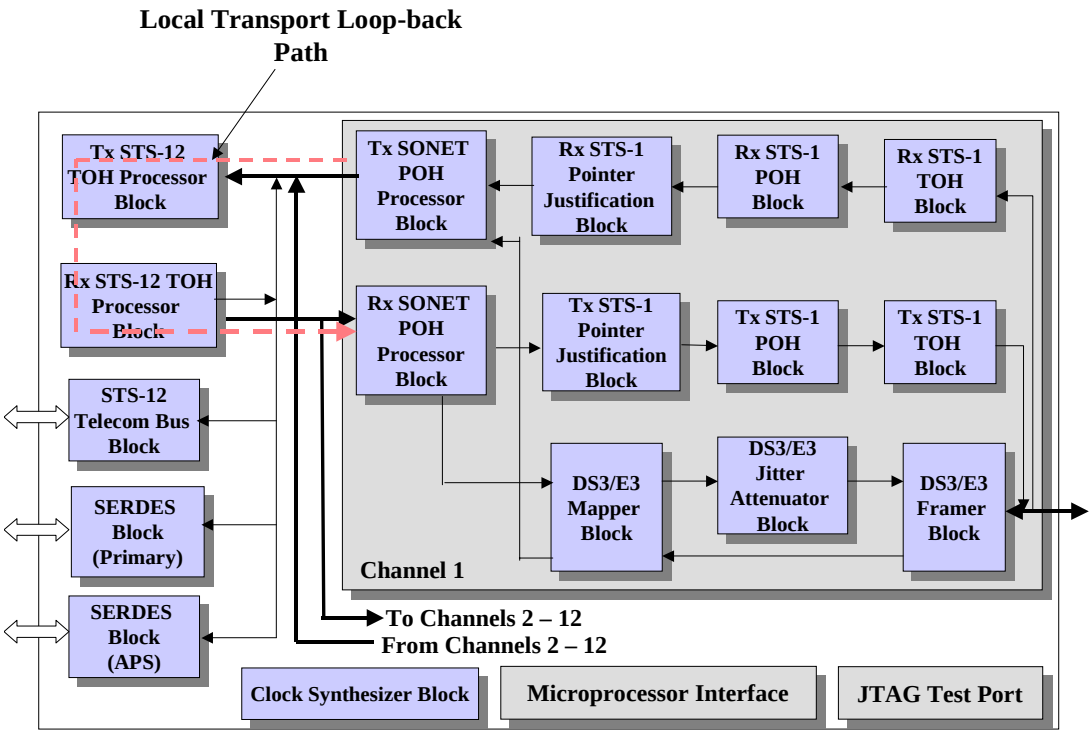

Figure 3-7, Illustration of the XRT94L43 device when configured to operate in the "Local Transport Loop-back" Mode

Q3.7: How does one configure the XRT94L43 device to operate in the "Local Path Loop-back" Mode?

A3.7: The user accomplishes this by executing the following steps.

STEP 1: Disable the "Auto AIS-P Downstream upon the various STS-12 Defect Conditions" features.

The user can accomplish this by executing the following two sub-steps.

STEP 1a. Writing the value "0x00" into the "Receive STS-12 Transport – Auto AIS Control Register" as depicted below.

Receive STS-12 Transport – Auto AIS Control Register (Indirect Address = 0x04, 0x63; Direct Address = 0x0563)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit AIS-P (Down-stream) Upon J0 Message Unstable	Transmit AIS-P (Down-stream) Upon J0 Message Mismatch	Transmit AIS-P (Down-stream) Upon SF	Transmit AIS-P (Down-stream) Upon SD	Transmit AIS-P (Down-stream) upon Loss of Optical Carrier AIS	Transmit AIS-P (Down-stream) upon LOF	Transmit AIS-P (Down-stream) upon LOS	Transmit AIS-P (Down-stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: If the user executes this step, then he/she will prevent the Receive STS-12 TOH Processor block from automatically transmitting the AIS-P indicator, in the downstream direction (towards the three Receive SONET POH Processor blocks) should it (the Receive STS-12 TOH Processor block) declare any of the above-mentioned defect conditions while attempting to execute "Local-Path" Loop-back.

STEP 1b: Writing the value "0x00" into the "Receive STS-12 Transport – Auto AIS (in Downstream STS-1s) Control Register, as depicted below.

Receive STS-12 Transport – Auto AIS (in Downstream STS-1s) Control Register (Indirect Address = 0x04, 0x6B; Direct Address = 0x056B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	Unused	Transmit AIS-P (via Downstream STS-1s) upon LOS	Transmit AIS-P (via Downstream STS-1s) upon LOF	Transmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	AIS-L Output Enable	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: If the user executes this step, then he/she will prevent each of the twelve (12) Transmit STS-1 TOH Processor block from automatically transmitting the AIS-P indicator, in the downstream direction (towards the DS3/E3/STS-1 LIU Devices) should the Receive STS-12 TOH Processor block declare any of the above-mentioned defect conditions while attempting to execute "Local-Path" Loop-back.

STEP 2 – Configure the XRT94L33 device to operate in the Local Path Loop-back Mode.

The user can accomplish this by writing the value "0x03" into the "Loop-back Control Register – Byte 0" as depicted below.

Loop-back Control Register – Byte 0 (Indirect Address = 0x00, 0x1F; Direct Address = 0x011F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				Loop-back[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

For the sake of completeness, an illustration of the XRT94L43 device, when configured to operate in the Local Path Loop-back Mode is presented below in Figure 3-8.

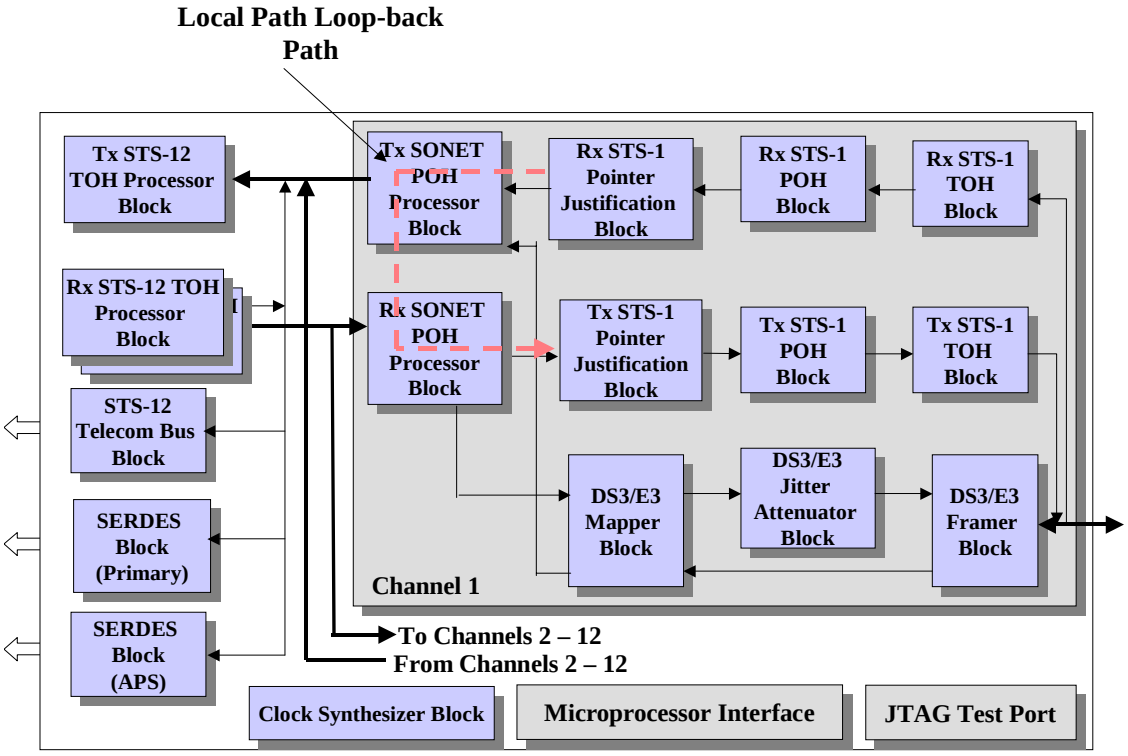

Figure 3-8, Illustration of the XRT94L43 device when configured to operate in the "Local Path Loop-back" Mode

Q3.8: How does one configure a given channel, within the XRT94L43 device to operate in the "STS-1 Local Loop-back" Mode?

A3.8: The user accomplishes this by setting Bit 5 (STS-1 Local Loop-back), within the "Mapper Control Register – Byte 2" to "1" as is depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 OH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	0	0	0	0

NOTE: The value "N" (within the Indirect Address value) ranges from "1" to "C" for each of the twelve channels.

For the sake of completeness, an illustration of the XRT94L43 device, when configured to operate in the "STS-1 Local Loop-back" Mode is presented below in Figure 3-9.

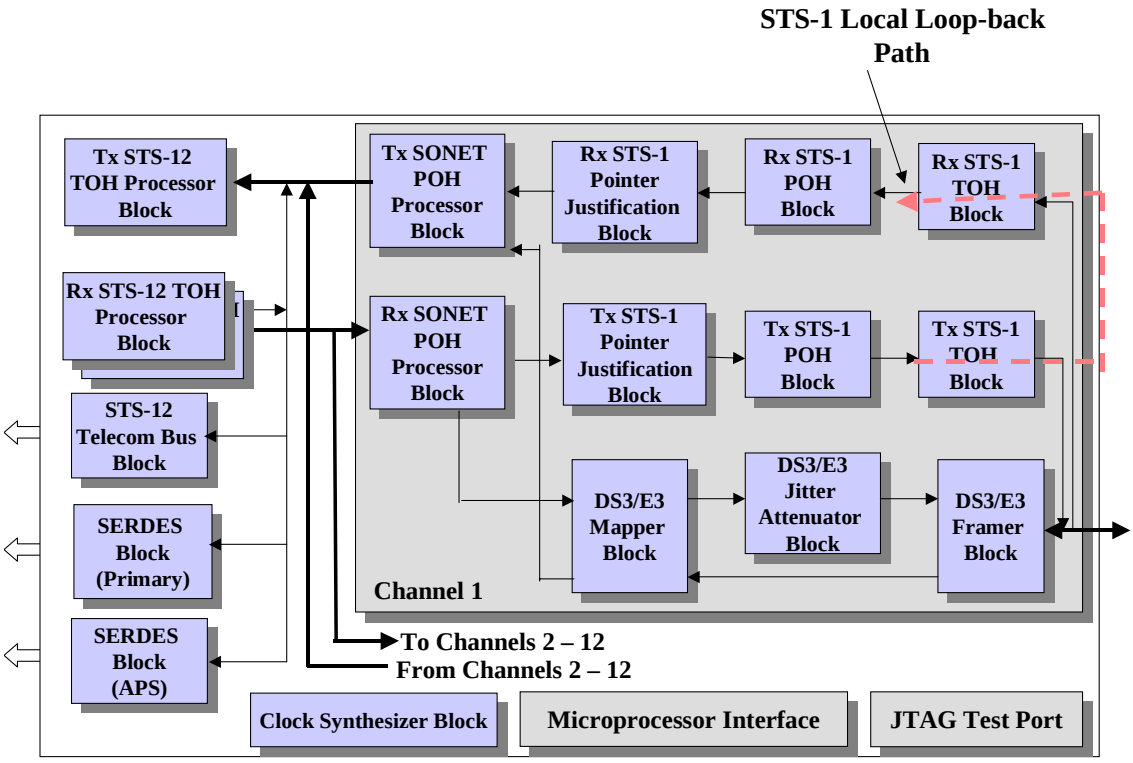

Figure 3-9, Illustration of the XRT94L43 device when configured to operate in the "STS-1 Local Loop-back" Mode

Q3.9: How does one configure a given channel, within the XRT94L43 device to operate in the "STS-1 Remote Loop-back" Mode?

A3.9: The user accomplishes this by setting Bit 6 (STS-1 Remote Loop-back), within the "Mapper Control Register – Byte 2" to "1" as is depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 OH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	0	0

NOTE: The value "N" (within the Indirect Address value) ranges from "1" to "C" for each of the twelve channels.

For the sake of completeness, an illustration of the XRT94L43 device, when configured to operate in the "STS-1 Remote Loop-back" Mode is presented below in Figure 3-10.

Frequently Asked Questions regarding the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/STM-4 Mapper IC

Preliminary

August 15, 2006

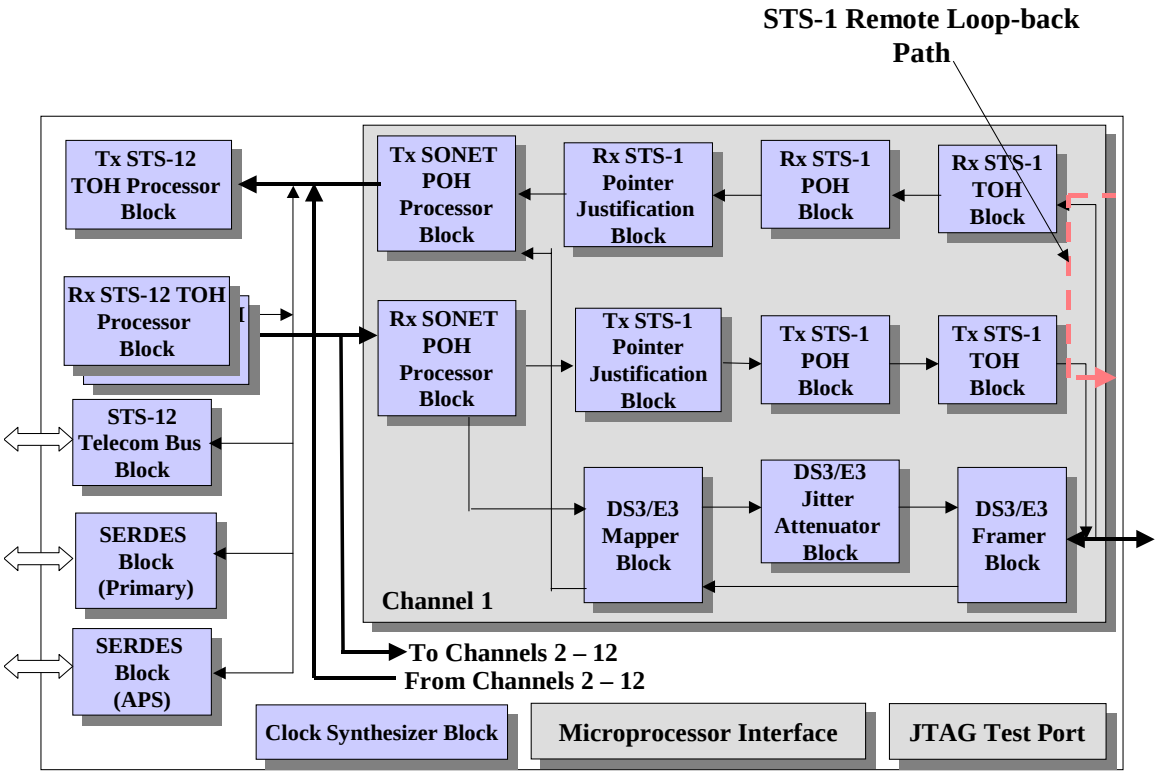

Figure 3-10, Illustration of the XRT94L43 device when configured to operate in the "STS-1 Remote Loop-back" Mode

Q3.10: How does one configure a given channel, (within the DS3/E3 Framer block) of the XRT94L43 device to operate in the "DS3/E3 Framer Local Loop-back" Mode?

A3.10: The user accomplishes this by setting Bit 7 (Local Loop-back), within the "Operating Mode Register" to "1" as is depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	1

NOTE: The value "N" (within the Indirect Address value) ranges from "1" to "C" for each of the twelve channels.

For the sake of completeness, an illustration of a given channel (within the XRT94L43 device) when configured to operate in the "DS3/E3 Framer Local Loop-back Mode" is presented below in Figure 3-11.

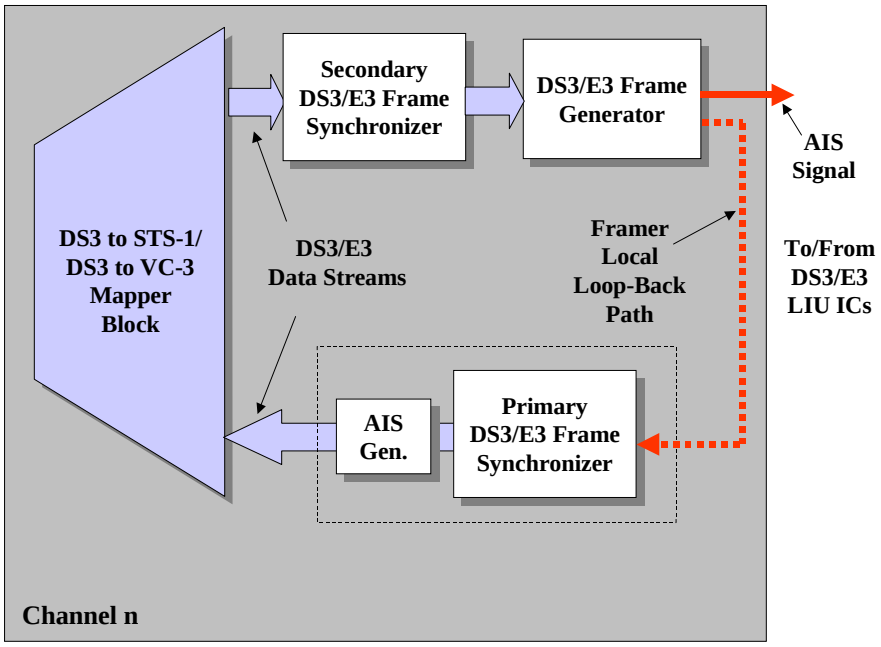

Figure 3-11, An Illustration of a given Channel (within the XRT94L43 device) when configured to operate in the "DS3/E3 Framer Local Loop-back" Mode

NOTE: Whenever a given channel has been configured to operate in the DS3/E3 Framer Local Loop-back Mode, then the Frame Generator block will (in addition to routing traffic to the receive input of the Primary Frame Synchronizer block) generate and transmit an AIS pattern via its output.

Q3.11: How does one configure a given channel (within the DS3/E3 Framer block) of the XRT94L43 device to operate in the "DS3/E3 Framer Remote Loop-back" Mode?

A3.11: The user accomplishes this by setting Bit 7 (Internal Remote Loop-back), within the "Line Interface Drive" Register to "1" as is depicted below.

Line Interface Drive Register (Indirect Address = 0xNE, 0x80; Direct Address = 0xNF80)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Internal Remote Loop-back	Unused	REQB Output Pin	TAOS Output Pin	ENCODIS Output Pin	TxLEV Output Pin	RLOOP Output Pin	LLOOP Output Pin
R/W	R/O	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	1	0	0	0

NOTE: The value "N" (within the Indirect Address value) ranges from "1" to "C" for each of the twelve channels.

For the sake of completeness, an illustration of a given channel (within the XRT94L43 device) when configured to operate in the "DS3/E3 Framer Internal Remote Loop-back" Mode is presented below in Figure 3-12.

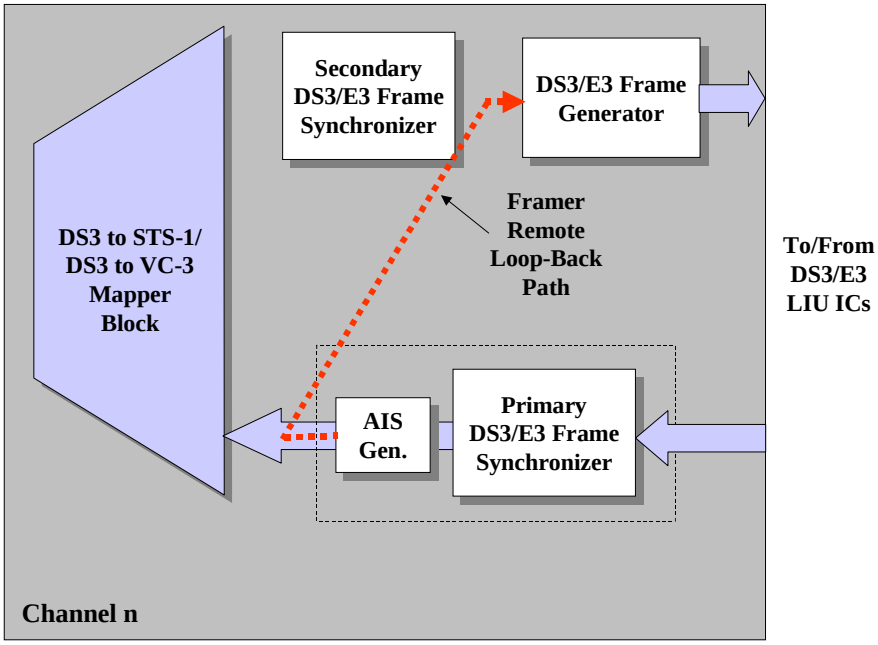

Figure 3-12, An Illustration of a given Channel (within the XRT94L43 device) when configured to operate in the "DS3/E3 Framer Internal Remote Loop-back" Mode

Q3.12: If the XRT94L43 Device has been configured to operate in the SDH Mode, can be configured to support the AU-3/VC-3 and the AU-4/TUG-3 Mapper Modes?

A3.12: Yes, if the XRT94L34 device has been configured to operate in the SDH Mode, then it can be configured to support either the AU-3/VC-3 or the AU-4/TUG-3 Mapper Mode. The user can accomplish this configuration selection by writing the appropriate value into Bits 3 through 0 within the "Mode Control Register – Byte 0" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	X	X	X	X

NOTE: The XRT94L43 device permits the user to support a "mix" of AU-3/VC-3 Mapping and AU-4/TUG-3 Mapper. In other words, the XRT94L43 device permits the user to configure some groups (of three VC-3 channels) into the AU-3/VC-3 Mapper Mode and other groups (of three VC-3 channels) into the AU-4/TUG-3 Mapper Mode.

Q3.13: Does the XRT94L43 device contain any BERT (Bit Error Rate Test) capability?

A3.13: Yes, each of the twelve DS3/E3 Frame Generator blocks contain a PRBS generator, and each of the twelve Primary DS3/E3 Frame Synchronizer blocks contain a PRBS receiver. Questions Q8.5 through Q8.7 provide additional information on how one can use this BERT capability within the DS3/E3 Framer block circuitry, in order to perform data-integrity checking within a given system.

NOTE: There is NO BERT capability within the SONET/SDH blocks.

Q3.14: How are the individual DS3, E3 or STS-1 Channels mapped into an STS-12 signal?

A3.14: Table 3-2 presents the "Mapping Relationship" between the individual DS3, E3 or STS-1 Channels (that are accepted by the XRT94L43 device, in the Ingress Direction) and the corresponding "STS-1 position" that they appear in, within the outbound STS-12 signal that is generated by the XRT94L43 device.

Table 3-2, The Mapping Relationship between the DS3/E3/STS-1 Input Channels and the corresponding "STS-1 Position" that they appear in, within the outbound STS-12 signal that is generated by the XRT94L43 device

DS3/E3/STS-1 Channel Number	STS-1 Position within the outbound STS-12 Signal
0	STS-1 # 1
1	STS-1 # 4
2	STS-1 # 7
3	STS-1 # 10
4	STS-1 # 2
5	STS-1 # 5
6	STS-1 # 8
7	STS-1 # 11
8	STS-1 # 3
9	STS-1 # 6
10	STS-1 # 9
11	STS-1 # 12

NOTE: Table 3-2 applies only if the XRT94L43 device is handling an STS-12 signal that contains 12 STS-1 (e.g., no STS-3c) signals.

Q3.15: How are the individual DS3 and E3 Channels mapped into an STM-4/TUG-3 signal?

A3.15: Table 3-3 presents the "Mapping Relationship" between the individual DS3 and E3 channels (that are accepted by the XRT94L43 device, in the Ingress Direction) and the corresponding "AU-4/TUG-3 position" that they appear in, within the outbound STM-4 signal that is generated by the XRT94L43 device.

Table 3-3, The Mapping Relationship between the DS3/E3 Input Channels and the corresponding "AU-4/TUG-3 positions" that they appear in, within the "outbound" STM-4 signal that is generated by the XRT94L43 device

DS3/E3 Channel Number	AU-4 Position within the outbound STM-4 Signal	VC-3 Position within the outbound AU-4 Signal
0	AU-4 # 1	VC-3 # 1
1	AU-4 # 2	VC-3 # 1
2	AU-4 # 3	VC-3 # 1
3	AU-4 # 4	VC-3 # 1
4	AU-4 # 1	VC-3 # 2
5	AU-4 # 2	VC-3 # 2
6	AU-4 # 3	VC-3 # 2
7	AU-4 # 4	VC-3 # 2
8	AU-4 # 1	VC-3 # 3
9	AU-4 # 2	VC-3 # 3
10	AU-4 # 3	VC-3 # 3
11	AU-4 # 4	VC-3 # 3

NOTE: Table 3-3 applies only if every channel within the XRT94L43 device was configured to operate in the STM-4/TUG-3 Mapping Mode (e.g., none of the AU-4 Blocks are configured to operate in the STM-4/AU-3 Mapping Mode).

Q4: Automatic Protection Switching (APS)-related Questions

Q4.1: What resources does the XRT94L43 device have to support APS?

A4.1: The XRT94L43 supports APS on the STS-12/STM-4 PECL Interface; in that (1) contains two sets of Receive STS-12 TOH Processor blocks (e.g., a "Primary" Receive STS-12 TOH Processor block, and a "Redundant" Receive STS-12 TOH Processor block). Each of these "Receive STS-12 TOH Processor" block, are "full-blown" Receive STS-12 TOH Processor blocks (they each have exactly the same set of registers and features). The XRT94L43 device also contains two sets (e.g., "Primary" and "Redundant") of the following pins.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins

Pin Name	Pin Number	Type	Description
RxLCLKL_P	M5	I	**Receive STS-12/STM-4 Clock – Positive Polarity PECL Input:** This input pin, along with RXL_CLKL_N functions as the Recovered Clock Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface Clock Input (for High-Speed Back-plane applications). The Receive STS-12/STM-4 PECL Interface Block will sample the data, applied at the "RXLDATA_P/RXLDATA_N" input pins, upon the falling edge of this signal. **NOTE:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_CLKL_N" functions as the "Primary Receive Clock Input" port. 2. The clock signal that is applied to this and the "RXL_CLKL_N" input pins will function as the clock/timing source for the Primary Receive STS-12 TOH Processor block.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
RxLCLKL_N	L5	I	**Receive STS-12/STM-4 Clock – Negative Polarity PECL Input:** This input pin, along with RXL_CLKL_P functions as the Recovered Clock Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface clock input (for High-Speed Back-plane applications). The Receiver STS-12/STM-4 PECL Interface Block will sample the data applied at the "RXLDATA_P/RXLDATA_N" input pins, upon the rising edge of this signal. **NOTE:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_CLKL_P" functions as the "Primary Receive Clock Input" Port. 2. The clock signal that is applied to this and the "RXL_CLKL_P" input pins, will function as the clock/timing source for the Primary Receive STS-12 TOH Processor block.
RxLCLKL_R_P	K2	I	**Receive STS-12/STM-4 Clock – Positive Polarity PECL Input – Redundant Port:** This input pin, along with RXL_CLKL_R_N functions as the Recovered Clock Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface Clock Input (for High-Speed Back-plane applications). The Receive STS-12/STM-4 PECL Interface Block will sample the data, applied at the "RXLDATA_R_P/RXLDATA_R_N" input pins, upon the falling edge of this signal. **NOTE:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_CLKL_R_N" functions as the "Redundant" Receive Clock Input Port. 2. The clock signal that is applied to this and the "RXL_CLKL_R_P" input pins, will function as the clock/timing source for the Redundant Receive STS-12 TOH Processor block.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
RxLCLKL_R_N	K1	I	**Receive STS-12/STM-4 Clock – Negative Polarity PECL Input – Redundant Port:** This input pin, along with RXL_CLKL_P functions as the Recovered Clock Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface Clock Input (for High-Speed Back-plane applications). The Receiver STS-12/STM-4 PECL Interface Block will sample the data applied at the "RXLDATA_R_P/RXLDATA_R_N" input pins, upon the rising edge of this signal. **NOTES:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_CLKL_R_ P" functions as the "Redundant" Receive Clock Input Port. 2. The clock signal that is applied to this and the "RXL_CLKL_R_P" input pins, will function as the clock/timing source for the Redundant Receive STS-12 TOH Processor block.
RxLDATA_P	K4	I	**Receive STS-12/STM-4 Data – Positive Polarity PECL Input:** This input pin, along with RXL_DATA_N functions as the Recovered Data Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface Data Input (for High-Speed Back-plane applications). The Receive STS-12/STM-4 PECL Interface block will sample the data applied to these input pins, upon the falling edge of the "RXL_CLKL_P" (and the rising edge of the "RXL_CLKL_N") signals. **NOTES:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_DATA_N" functions as the "Primary" Receive Data Input Port. 2. Data that is applied to this and the "RXL_DATA_N" input pins, will be routed to, and processed by the Primary Receive STS-12 TOH Processor block.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
RxLDATA_N	L4	I	**Receive STS-12/STM-4 Data – Negative Polarity PECL Input:** This input pin, along with RXL_DATA_P functions as the Recovered Data Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface Data Input (for High-Speed Back-plane applications). The Receive STS-12/STM-4 PECL Interface block will sample the data applied to these input pins, upon the falling edge of the "RXL_CLKL_P" (and the rising edge of the "RXL_CLKL_N") signals. **NOTES:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_DATA_P" functions as the "Primary Receive Data Input Port". 2. Data that is applied to this and the "RXL_DATA_P" input pins, will be routed to, and processed by the Primary Receive STS-12 TOH Processor block.
RxLDATA_R_P	K3	I	**Receive STS-12/STM-4 Data – Positive Polarity PECL Input – Redundant Port:** This input pin, along with "RXL_DATA_R_N" functions as the Recovered Data Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface Data Input (for High-Speed Back-plane applications). The Receive STS-12/STM-4 PECL Interface block will sample the data applied to these input pins, upon the falling edge of the "RXL_CLKL_R_P" (and the rising edge of the "RXL_CLKL_R_N") signals. **NOTE:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_DATA_R_N" functions as the "Redundant Receive Data Input Port". 2. Data that is applied to this and the "RXL_DATA_R_N" input pins, will be routed to, and processed by the Redundant Receive STS-12 TOH Processor block.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
RxLDATA_R_N	L3	I	**Receive STS-12/STM-4 Data – Negative Polarity PECL Input – Redundant Port:** This input pin, along with "RXL_DATA_R_P" functions as the Recovered Data Input, from the Optical Transceiver or as the Receive STS-12 PECL Interface Data Input (for High-Speed Back-plane applications). The Receive STS-12/STM-4 Interface block will sample the data applied to these input pins, upon the falling edge of the "RXL_CLKL_R_P" (and the rising edge of the "RXL_CLKL_R_N") signals. **NOTE:** 1. For APS (Automatic Protection Switching) purposes, this input pin, along with "RXL_DATA_R_N" functions as the "Redundant Receive Data Input Port". 2. Data that is applied to this and the "RXL_DATA_R_N" input pins, will be routed to, and processed by the Redundant Receive STS-12 TOH Processor block.
TxLCLKO_P	M1	O	**Transmit STS-12/STM-4 Clock – Positive Polarity PECL Output:** This output pin, along with TXL_CLKO_N functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the "TXL_DATA_P/TXL_DATA_N" output pins upon the rising edge of this clock signal. **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_CLKO_N" functions as the "Primary Transmit Output Clock" signal.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
TxLCLKO_N	M2	O	**Transmit STS-12/STM-4 Clock – Negative Polarity PECL Output:** This output pin, along with TXLCLKO_P functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the "TXL_DATA_P/TXL_DATA_N" output pins upon the falling edge of this clock signal. **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_CLKO_N" functions as the "Primary Transmit Output Clock" signal.
TxLCLKO_R_P	R1	O	**Transmit STS-12/STM-4 Clock – Positive Polarity PECL Output – Redundant Port:** This output pin, along with TXL_CLKO_R_N functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the "TXL_DATA_R_P/TXL_DATA_R_N" output pins upon the rising edge of this clock signal. **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_CLKO_R_N" functions as the "Redundant Transmit Output Clock" signal.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
TxLCLKO_R_N	R2	O	**Transmit STS-12/STM-4 Clock – Negative Polarity PECL Output – Redundant Port:** This output pin, along with TXL_CLKO_R_P functions as the Transmit Clock Output signal. These output pins are typically used in "High-Speed" Back-Plane Applications. In this case, outbound STS-12/STM-4 data is output via the "TXL_DATA_R_P/TXL_DATA_R_N" output pins upon the rising edge of this clock signal. **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_CLKO_R_P" functions as the "Redundant Transmit Output Clock" signal.
TxLDATA_P	N1	O	**Transmit STS-12/STM-4 Data - Positive Polarity PECL Output:** This output pin, along with TXL_DATA_N functions as the Transmit Data Output, to the Optical Transceiver. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXL_CLKO_P/TXL_CLKO_N"). **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_DATA_N" functions as the "Primary" Receive Data Input Port.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
TxLDATA_N	N2	O	**Transmit STS-12/STM-4 Data – Negative Polarity PECL Output:** This output pin, along with TXL_DATA_P functions as the Transmit Data Output, to the Optical Transceiver. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of TXL_CLKO_P/TXL_CLKO_N). **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_DATA_P" functions as the "Primary" Receive Data Input Port.
TxLDATA_R_P	P1	O	**Transmit STS-12/STM-4 Data - Positive Polarity PECL Output - Redundant Port:** This output pin, along with TXL_DATA_R_N functions as the Transmit Data Output, to the Optical Transceiver. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXL_CLKO_R_P/TXL_CLKO_R_N"). **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_DATA_N" functions as the "Redundant" Receive Data Input Port.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
TxLDATA_R_N	P2	O	**Transmit STS-12/STM-4 Data - Negative Polarity PECL Output - Redundant Port:** This output pin, along with TXL_DATA_R_P functions as the Transmit Data Output, to the Optical Transceiver. For "High-Speed" Back-Plane Applications, the user should note that data is output from these output pins upon the rising/falling edge of "TXL_CLKO_R_P/TXL_CLKO_R_N"). **NOTE:** For APS (Automatic Protection Switching) purposes, this output pin, along with "TXL_DATA_R_P" functions as the "Redundant" Receive Data Input Port.
LOS	AF6	I	**Loss of Optical Carrier Input – Primary:** The user is expected to connect the "Loss of Carrier" output (from the Optical Transceiver) to this input pin. If this input pin is pulled "high", then the Primary Receive STS-12 TOH Processor block will declare a "Loss of Optical Carrier" condition. **NOTE:** This input pin is only active if the "Primary Port" is active. This input pin is inactive if the "Redundant Port" is active.

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
LOS_R	AE6	I	**Loss of Optical Carrier Input – Redundant:** The user is expected to connect the "Loss of Carrier" output (from the Optical Transceiver) to this input pin. If this input pin is pulled "high", then the Redundant Receive STS-12 TOH Processor block will declare a "Loss of Optical Carrier" condition. **NOTE:** This input pin is only active if the "Redundant Port" is active. This input pin is inactive if the "Primary Port" is active.
EXSWITCH	AB7	O	**External (APS) Switch Output Pin:** This output pin can used to permit the XRT94L43 device to perform APS externally. Specifically, this output pin can be connected to some circuitry that permits the re-direction of STS-12/STM-4 traffic, should an APS event be needed. **NOTE:** This output pin is disabled if the "EXSWITCHDIS" input pin (pin number AB6) is pulled "HIGH".

Table 4-1, Listing of STS-12/STM-4 PECL Interface Pins (Continued)

Pin Name	Pin Number	Type	Description
EXSWITCH DISABLE	AB6	I	**External (APS) Switch Disable:** This input pin permits the user to configure the XRT94L43 device to perform APS internally or externally. 0 – Configures the XRT94L43 to perform APS externally. In this mode, the XRT94L43 device will execute an APS by toggling the state of the "EXSWITCH" output pin. 1 – Configures the XRT94L43 device to perform APS internally. In this mode, the XRT94L43 device will internally switch from using the "Primary" port to the "Redundant" port (or vice-versa).

In addition to the "above-mentioned" pins, the XRT94L43 device also comes with the "STS-12 Line APS Control" Register, which permits the user to configure the APS Controller, as appropriate. The bit-format and description of each register bit is presented below.

STS-12 Line APS Control Register (Indirect Address = 0x00, 0x80; Direct Address = 0x0180)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused					Port In Use	APS Auto Switch Enable	APS Switch
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit Number	Name	Type	Description
7 – 3	Unused	R/O	
2	Port In Use	R/O	**Port In Use – Identifier:** This READ-ONLY bit-field indicates which port that the XRT94L43 device is using to receive the incoming STS-12/STM-4 signal, as described below. **0 – Primary Receive STS-12/STM-4 PECL Interface Input Port is in use.** In this mode, the XRT94L43 device is receiving the incoming STS-12/STM-4 signal via the Primary Receive PECL Interface Port. More specifically, this means that each of the 12 Receive SONET POH Processor blocks are now receiving their corresponding STS-1 SPE data from the Primary Receive STS-12 TOH Processor block. **1 – Back-up (Redundant) Receive STS-12/STM-4 PECL Interface Port is in use.** In this mode, the XRT94L43 device is receiving the incoming STS-12/STM-4 signal via the Redundant Receive PECL Interface. More specifically, this means that each of the 12 Receive SONET POH Processor blocks are now receiving their corresponding STS-1 SPE data form the Redundant Receive STS-12 TOH Processor block **NOTE:** This bit-field is not active if the "STS-12/STM-4 Telecom Bus Interface is enabled.

STS-12 Line APS Control Register – Bit-field Description (Continued)

Bit Number	Name	Type	Description
1	APS Auto Switch Enable	R/W	**APS Auto Switch Enable:** This READ/WRITE bit-field permits the user to configure the XRT94L43 device to automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STS-12 TOH Processor block declares an LOS (Loss of Signal) defect condition. 0 – Disables the APS Auto Switch feature. In this mode, the XRT94L43 will not automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STS-12 TOH Processor block declares the LOS defect condition. 1 – Enables the APS Auto Switch feature **NOTES:** 1. This bit-field is not active if the "STS-12/STM-4 Telecom Bus Interface is enabled. 2. The XRT94L43 device only supports this "APS upon LOS" switching from the "Primary" to the "Redundant" port. It does not support "Revertive" switching. In other words, there will be no automatic switching from the Redundant back to the Primary Port if the Redundant Receive STS-12 TOH Processor block were to declare the LOS defect condition., 3. The XRT94L43 device only supports APS switching in the event the Receive STS-12 TOH Processor block declares the LOS defect condition. Software control is needed to support APS, in the event of the Primary Receive STS-12 TOH Processor block declaring LOF, AIS-L, SD or SF, etc.

STS-12 Line APS Control Register – Bit-field Description (Continued)

Bit Number	Name	Type	Description
0	APS Switch	R/W	**APS Switch Command:** This READ/WRITE bit-field permits the user to command an APS switch (from one port to the other) via software control. 0 – Configures each of the 12 Receive SONET POH Processor blocks to use the "Primary Receive STS-12 TOH Processor block as the source for their incoming STS-1 SPE data 1 – Configures each of the 12 Receive SONET POH Processor blocks to use the "Redundant Receive STS-12 the Receive STS-12 TOH Processor block to use the "Redundant Receive STS-12 TOH Processor block" as the source for their incoming STS-1 SPE data. **NOTE:** This bit-field is not active if the "STS-12/STM-4 Telecom Bus Interface is enabled.

NOTE: APS is supported only supported on the STS-12/STM-4 PECL Interface. APS is NOT supported on the STS-12/STM-4 Telecom Bus Interface block.

Q4.2: What is going on within the XRT94L43 device, when one implements APS?

A4.2: The XRT94L43 consists of two sets of the following.

- Receive STS-12/STM-4 PECL Interface Input pins
  - The Primary Receive STS-12/STM-4 PECL Interface Input pins
  - The Redundant Receive STS-12/STM-4 PECL Interface Input pins
- Transmit STS-12/STM-4 PECL Interface Output pins
  - The Primary Transmit STS-12/STM-4 PECL Interface Output pins
  - The Redundant Transmit STS-12/STM-4 PECL Interface Output pins
- Receive STS-12 TOH Processor Blocks
  - The Primary Receive STS-12 TOH Processor block
  - The Redundant Receive STS-12 TOH Processor block

In order to fully understand the "APS" system within the XRT94L43 device, the user should refer to Figure 4-1 below.

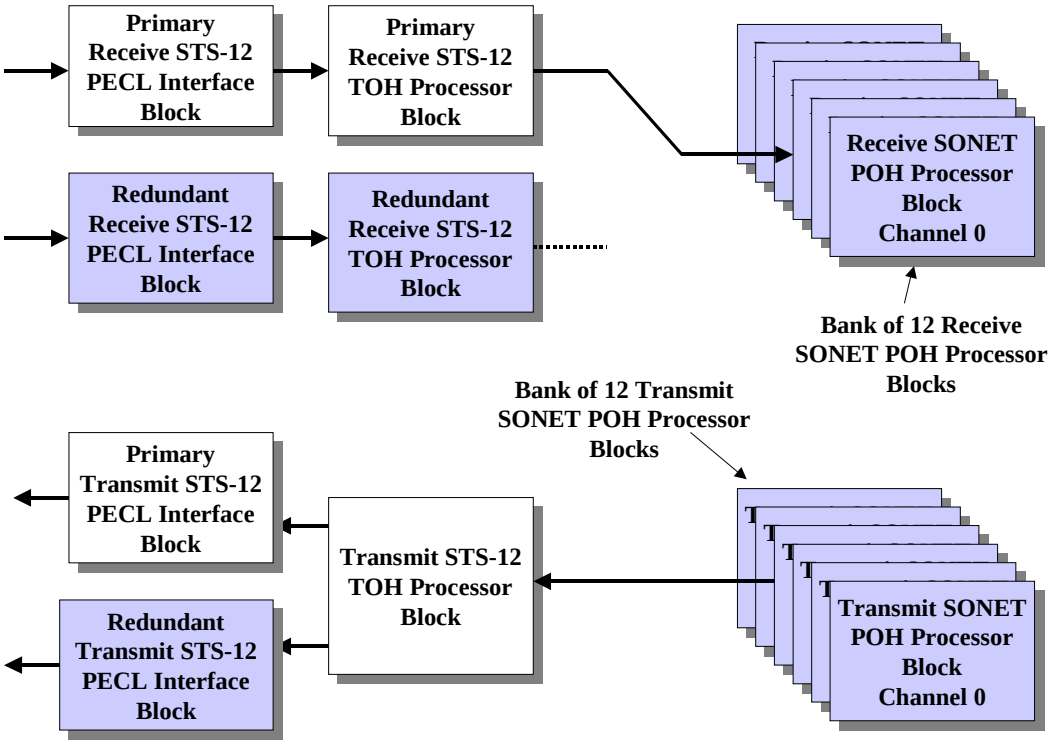

Figure 4-1, Illustration of the "APS" System within the XRT94L43 device

Figure 4-1 presents an illustration of the APS System within the XRT94L43 device. The following text will discuss the role of each of the functional blocks within this figure.

In the Transmit Direction

In the Transmit Direction, outbound STS-1 SPE signals (originating from the 12 Transmit SONET POH Processor blocks) will be routed to the Transmit STS-12 TOH Processor block. The Transmit STS-12 TOH Processor block will take each of these 12 STS-1 SPE data-stream, and will (1) byte-interleave all of the outbound STS-1 data into an STS-12 signal, and (2) compute and insert the TOH bytes within this outbound STS-12 data-stream.

As the Transmit STS-12 TOH Processor outputs this STS-12 data, it actually routes this data (in parallel) to the following two different blocks.

- The Primary Transmit STS-12/STM-4 PECL Interface Block
- The Redundant Transmit STS-12/STM-4 PECL Interface Block

As a consequence, both the Primary Transmit STS-12/STM-4 PECL Interface and the Redundant STS-12/STM-4 PECL Interface blocks will each accept and output the exact same set of STS-12/STM-4 data simultaneously.

NOTE: Both the Primary and the Redundant Transmit STS-12/STM-4 PECL Interface blocks will ALWAYS output the same (e.g., identical) set of STS-12/STM-4 data regardless of the state of the "APS Switch" bit, that will be discussed later.

In the Receive Direction

In the case of the Receive Direction, the Primary and Redundant Receive STS-12/STM-4 PECL Interface blocks will each be capable of receiving their own incoming STS-12/STM-4 signal. Afterwards, each of these incoming STS-12/STM-4 signals will be routed to their corresponding Receive STS-12 TOH Processor block. More specifically, the STS-12/STM-4 signal that is received by the Primary Receive STS-12/STM-4 PECL Interface block will be routed to the Primary Receive STS-12 TOH Processor block for further processing. Likewise, the STS-12/STM-4 signal that is received by the Redundant Receive STS-12/STM-4 PECL Interface block will be routed to the Redundant Receive STS-12 TOH Processor block for further processing.

The role that the Primary and Redundant Receive STS-12 TOH Processor blocks play on these incoming STS-12/STM-4 signals are identical with each other. Each of these blocks will perform the following functions on their respective incoming STS-12/STM-4 signals.

- To acquire and maintain framing with the incoming STS-12/STM-4 signal
- To compute and verify the B1 and B2 bytes within the TOH of the incoming STS-12 data-stream
- To increment the PMON B1 Byte Error Count Register each time the Receive STS-12 TOH Processor block detects a B1 byte error.
- To increment the PMON B2 Byte Error Count Register each time the Receive STS-12 TOH Processor block detects a B2 byte error.
- To flag and declare the following defect conditions: LOS, LOF, AIS-L, SD, SF, RDI-L and Section Trace Message Mismatch.
- To (optionally) automatically transmit the AIS-P indicator in the down-stream direction (towards the 12 Receive SONET POH Processor blocks) whenever (and for the duration that) the Receive STS-12 TOH Processor Block declares any of the following defect conditions: LOS, LOF, AIS-L and Section Trace Message Mismatch.
- To detect the occurrence of REI-L events and to increment the PMON REI-L Event Count Register, each time these events are detected.

- To byte-de-interleave the incoming STS-12 signal into to 12 STS-1 signal and to (if configured) route these STS-1 signals to each of the 12 Receive SONET POH Processor blocks

The XRT94L43 device consists of 12 Receive SONET POH Processor blocks that are only capable of receiving their STS-1 data-stream from one "Receive STS-12 TOH Processor Block" at any given time. In other words, this bank of 12 Receive SONET POH Processor blocks can only be configured to receive all of their STS-1 data from the Primary Receive STS-12 TOH Processor block or they can be configured to receive all of their STS-1 data from the Redundant Receive STS-12 TOH Processor block. The 12 Receive SONET POH Processor blocks cannot be configured to receive all of their STS-1 data from both of these blocks. Further, the 12 Receive SONET POH Processor blocks cannot be configured to receive their STS-1 data from a "mixture" of the two Receive STS-12 TOH Processor blocks.

Whenever an APS event occurs (either upon Software Control, or automatically upon the Primary Receive STS-12 TOH Processor block declaring the LOS defect condition) what is actually happening is that the "bank of 12 Receive SONET POH Processor blocks" abruptly switches from receiving their STS-1 data from one (say the Primary) Receive STS-12 TOH Processor block, and now begin to receive their STS-1 data from the Redundant Receive STS-12 TOH Processor block.

Whenever the "bank of 12 Receive SONET POH Processor blocks" are configured to receive their STS-1 data from the "Primary" Receive STS-12 TOH Processor block, then that data which is being processed by the "Redundant" Receive STS-12 TOH Processor block will NOT be processed any further by the XRT94L43 device. However, the user is able to perform full Performance Monitoring on the STS-12/STM-4 signal that is being applied to the Redundant Receive STS-12 TOH Processor block. In other words, the user can still poll and interrogate the registers (associated with the Redundant Receive STS-12 TOH Processor block) and have a complete understanding of the quality of this particular STS-12 signal (e.g., the defects being declared, the number of B1 or B2 byte errors being detected, etc.). This ability permits the user to determine the quality of this particular STS-12 signal, prior to switching to this signal, in the event of an APS event.

Likewise, if the "bank of 12 Receive SONET POH Processor blocks" are configured to receive their STS-1 data from the "Redundant" Receive STS-12 TOH Processor block, then that data which is being processed by the "Primary" Receive STS-12 TOH Processor block will NOT be processed any further by the XRT94L43 device. However, the user is able to perform full Performance Monitoring on the STS-12/STM-4 signal that is being applied to the Primary Receive STS-12 TOH Processor block. In other words, the user

can still poll and interrogate the registers (associated with the Primary Receive STS-12 TOH Processor Block) and have a complete understanding of the quality of this particular STS-12 signal (e.g., the defects being declared, the number of B1 or B2 byte errors being detected, etc.).

NOTE: It is entirely possible that the Primary Port (consisting of the Primary Receive STS-12/STM-4 PECL Interface and the Primary Receive STS-12 TOH Processor blocks) is handling and processing an STS-12/STM-4 signal that is carrying different data than that being processed by the Redundant Port (consisting of the Redundant Receive STS-12/STM-4 PECL Interface and the Redundant Receive STS-12 TOH Processor blocks).

Q4.3 How does one configure the XRT94L43 device to automatically perform APS in the event of an LOS condition?

A4.3. The user can accomplish this by doing all of the following.

a. The user must interface the XRT94L43 device to two separate optical transceivers or back-plane interfaces. One Optical Transceiver or back-plane interface (deemed to be the "Primary Optical Transceiver") should be connected to the following pins.

- RxLCLKL_P
- RxLCLKL_N
- RxLDATA_P
- RxLDATA_N
- TxLCLKO_P
- TxLCLKO_N
- TxLDATA_P
- TxLDATA_N
- LOS

The other Optical Transceiver or back-plane interface (deemed to be the "Redundant Optical Transceiver") should be connected to the following pins.

- RxLCLKL_R_P
- RxLCLKL_R_N
- RxLDATA_R_P
- RxLDATA_R_N
- TxLCLKO_R_P
- TxLCLKO_R_N
- TxLDATA_R_P
- TxLDATA_R_N
- LOS_R

b. Next, the user should pull the EXSWITCH_DISABLE input pin (pin AB6) to a logic "HIGH". This step will configure the XRT94L43 to be capable of performing "internal" APS switching.

c. Afterwards, the user should set Bit 1 (APS Auto Switch Enable), within the "STS-12 Line APS Control" Register to "1", as illustrated below.

STS-12 Line APS Control Register (Indirect Address = 0x00, 0x80; Direct Address = 0x0180)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused					Port In Use	APS Auto Switch Enable	APS Switch
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	1	0

This step configures each of the 12 Receive SONET POH Processor block (within the XRT94L43 device) to automatically switch from receiving their incoming STS-1 SPE data via the "Primary" Receive STS-12 TOH Processor block to receiving their incoming STS-1 SPE data via the "Redundant" Redundant Receive STS-12 TOH Processor block; whenever the Primary Receive STS-12 TOH Processor block declares the LOS defect condition.

c. Finally, the user must set Bit 0 (APS Switch) within the "STS-12 Line APS Control" Register to "0" as indicated below.

STS-12 Line APS Control Register (Indirect Address = 0x00, 0x80; Direct Address = 0x0180)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused					Port In Use	APS Auto Switch Enable	APS Switch
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	X	1	0

This step configures each of the 12 Receive SONET POH Processor blocks (within the XRT94L43 device) to use the "Primary Receive STS-12 TOH Processor block" as their source for receiving their corresponding incoming STS-1 SPE data.

Once the user has executed these "above-mentioned" steps, then the XRT94L43 device will also now be configured to automatically implement APS (e.g., each of the 12 Receive SONET POH Processor block will automatically switch from accepting their incoming STS-1 SPE data from the Primary Receive STS-12 TOH Processor block to accepting their incoming STS-1 SPE from the Redundant Receive STS-12 TOH Processor block - as described per Question Q4.2), whenever the Primary Receive STS-12 TOH Processor block declares the LOS defect condition.

NOTES ABOUT THE APS CONTROLLER WITHIN THE XRT94L43 DEVICE

The APS Controller only supports "Automatic Switching" in the event that the Primary Receive STS-12 TOH Processor block declares the LOS defect

condition. It cannot be configured to support "Automatic Switching" upon the Primary Receive STS-12 TOH Processor block declaring the SD, SF, LOF or AIS-L defect conditions. This will have to be accomplished via Software control.

The APS Controller only supports "Automatic Switching upon LOS" from the "Primary" to the "Redundant" port. In other words, each of the 12 Receive SONET POH Processor blocks can be configured to automatically switch from receiving their STS-1 SPE data from the Primary Receive STS-12 TOH Processor block, to now receiving their STS-1 SPE data from the Redundant Receive STS-12 TOH Processor block, whenever the Primary Receive STS-12 TOH Processor block declares the LOS defect condition. The APS Controller does not support "Revertive" switching (e.g., from the "Redundant" port, back to the "Primary" port). In other words, each of the 12 Receive SONET POH Processor blocks CANNOT be configured to automatically switch from receiving their STS-1 SPE data from the Redundant Receive STS-12 TOH Processor block, to now receiving their STS-1 SPE data the Primary Receive STS-12 TOH Processor block, whenever the Redundant Receive STS-12 TOH Processor block declares the LOS defect condition.

Q4.4 Is there a way to determine whether the XRT94L43 device is processing the incoming STS-12 data that is being applied to the Primary or the Redundant Receive STS-12/STM-4 PECL Interface port?

A4.4: Yes, this can be accomplished by testing the state of Bit 2 (Port In Use), within the STS-12 Line APS Control Register (as depicted below).

STS-12 Line APS Control Register (Indirect Address = 0x00, 0x80; Direct Address = 0x0180)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused					Port In Use	APS Auto Switch Enable	APS Switch
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	X	1	X

If this bit-field is "0", then the XRT94L43 device is processing the STS-12/STM-4 signal that is being applied to the Primary STS-12/STM-4 PECL Interface port. In other words, each of the 12 Receive SONET POH Processor blocks are currently receiving their STS-1 SPE data from the Primary Receive STS-12 TOH Processor block. Conversely, if this bit-field is "1", then the XRT94L43 device is processing STS-12/STM-4 signal that is being applied to the Redundant Receive STS-12/STM-4 PECL Interface port. In other words, each of the 12 Receive SONET POH Processor blocks are currently receiving their STS-1 SPE data from the Redundant Receive STS-12 TOH Processor block.

Q4.5: Are both the "Primary" and "Redundant" Transmit PECL Clock and Data Output signals always active?

A4.5: Yes, the XRT94L43 device will be transmitting the "outbound" STS-12/STM-4 data via both the "Primary" and "Redundant" Transmit PECL output ports. There is no ability to disable one or both of these Transmit Output ports.

Q4.6 If the XRT94L43 device is current processing the incoming STS-12/STM-4 signal that is being applied to the "Primary Receive STS-12/STM-4 PECL Interface" port, can the XRT94L43 device monitor the state of the STS-12/STM-4 signal that is being applied to the "Redundant Receive STS-12/STM-4 PECL Interface" port?

A4.6: Yes, the XRT94L43 device provides full monitoring capability of the "Redundant Receive STS-12/STM-4 PECL Interface" port.

SOME THINGS TO BE AWARE OF:

1. If the XRT94L43 device is receiving an STS-12/STM-4 signal via the Primary Receive STS-12/STM-4 PECL Interface" port, then the XRT94L43 does permit the user to also monitor the quality of the STS-12/STM-4 signal that is being received via the "Redundant Receive STS-12/STM-4 PECL Interface" port.
    a. The user can obtain status information on the Primary STS-12/STM-4 signal by reading the contents of the Primary Receive STS-12 TOH Processor block registers (Indirect Address = 0x04, 0x00 through 0x04, 0x7F; Direct Address = 0x0500 through 0x057F)
    b. The user can obtain status information on the Redundant STS-12/STM-4 signal by reading the contents of the Redundant Receive STS-12 TOH Processor block registers (Indirect Address = 0x0C, 0x00 through 0x0C, 0x7F; Direct Address = 0x0D00 through 0x0D7F)
2. If an APS event is commanded (such that the XRT94L43 device is now processing the STS-12/STM-4 signal that is being applied to the Redundant STS-12/STM-4 PECL Interface" port), then the XRT94L43 device will still permit the user to monitor the quality of STS-12/STM-4 signal that is applied to the "Primary Receive STS-12/STM-4 PECL Interface" port.

Q4.7: How does one configure the XRT94L43 to perform APS (Automatic Protection Switching) under software control?

A4.7: The user can accomplish this by performing the following steps.

STEP 1 – Make sure that the EXSWITCH_DISABLE input pin (pin AB6) is pulled to a logic "HIGH".

STEP 2 – Wait for the Primary Receive STS-12 TOH Processor block to declare some defect condition, such as SD, SF, LOF, AIS-L or Section Trace Message Mismatch

STEP 3 – Once the Primary Receive STS-12 TOH Processor block has declared one of the "above-mentioned" defect condition, then set Bit 0 (APS Switch), within the "STS-12/STM-4 Line APS Control" Register, to "1" as depicted below.

STS-12 Line APS Control Register (Indirect Address = 0x00, 0x80; Direct Address = 0x0180)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused					Port In Use	APS Auto Switch Enable	APS Switch
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0 →1

Once the user executes this step, then the XRT94L43 device will begin to process the STS-12/STM-4 data that is being applied to the Redundant Receive STS-12/STM-4 PECL Interface.

NOTE: The user can confirm that the XRT94L43 device is now processing the data the data that is being applied to the "Redundant Receive STS-12/STM-4 PECL Interface" by reading out the contents of the "STS-12 Line APS Control" Register. If the user reads out the value "0x05" (e.g., where both Bits 2 and 0) are set to "1" as depicted below, then the XRT94L43 device has been configured to process the STS-12/STM-4 data that is being applied to the Redundant Receive STS-12/STM-4 PECL Interface.

STS-12 Line APS Control Register (Indirect Address = 0x00, 0x80; Direct Address = 0x0180)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused					Port In Use	APS Auto Switch Enable	APS Switch
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	1	0	1

Q4.8: If the XRT94L43 has gone through an APS (Automatic Protection Switching) event, can the XRT94L43 device still monitor the state of the STS-12/STM-4 signal that being received via the "Primary Receive STS-12/STM-4 PECL Interface" port?

A4.8: Yes, once the XRT94L43 has gone through an APS event (such that it is now receiving and processing the STS-12/STM-4 data that it is receiving via the "Redundant Receive STS-12/STM-4 PECL Interface" block), then the user can still monitor the state of the STS-12/STM-4 signal that is being received via the Primary Receive STS-12/STM-4 PECL Interface" block.

Q5: 4-Channel STS-3 to STS-12 Mapper-Related Questions

Q5.1: How does one configure the XRT94L43 device to operate in the "4-Channel STS-3 to STS-12 Mapper" Mode?

A5.1: The user can configure the XRT94L43 device to operate in the "4-Channel STS-3 to STS-12 Mapper' Mode, by executing the following four steps.

STEP 1 – Set Bit 7 (STS-3 Telecom Bus ON # 3), within the "Interface Control Register – Byte 3 – STS-3 Telecom Bus 3) to "1" as depicted below.

Interface Control Register – Byte 3 – STS-3 Telecom Bus 3 (Indirect Address = 0x00, 0x38; Direct Address = 0x0138)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 3	STS-3 Telecom Bus Tri-State # 3	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 3	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	1

This step enables STS-3 Telecom Bus Interface # 3.

STEP 2 – Set Bit 7 (STS-3 Telecom Bus ON # 2), within the "Interface Control Register – Byte 2 – STS-3 Telecom Bus 2) to "1" as depicted below.

Interface Control Register – Byte 2 – STS-3 Telecom Bus 2 (Indirect Address = 0x00, 0x39; Direct Address = 0x0139)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 2	STS-3 Telecom Bus Tri-State # 2	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 2	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

This step enables STS-3 Telecom Bus Interface # 2.

STEP 3 – Set Bit 7 (STS-3 Telecom Bus ON # 1), within the "Interface Control Register – Byte 1 – STS-3 Telecom Bus 1) to "1" as depicted below.

Interface Control Register – Byte 1 – STS-3 Telecom Bus 1 (Indirect Address = 0x00, 0x3A; Direct Address = 0x013A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 1	STS-3 Telecom Bus Tri-State # 1	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 1	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity ODD	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

This step enables STS-3 Telecom Bus Interface # 1.

STEP 4 – Set Bit 7 (STS-3 Telecom Bus ON # 1), within the "Interface Control Register – Byte 0 – STS-3 Telecom Bus 0) to "1" as depicted below.

Interface Control Register – Byte 0 – STS-3 Telecom Bus 0 (Indirect Address = 0x00, 0x3B; Direct Address = 0x013B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 0	STS-3 Telecom Bus Tri-State # 0	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 0	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

Once the user executes these four steps, then the resulting functional block diagram will be as illustrated below.

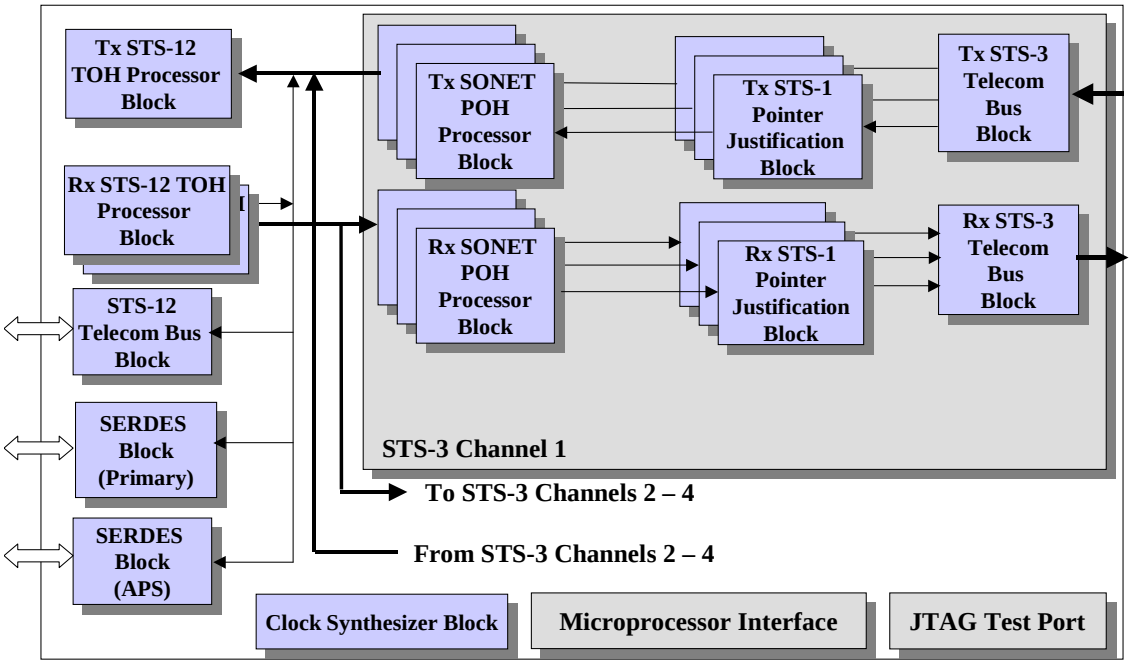

Figure 5-1, Functional Block Diagram of the XRT94L43 device, when it is configured to operate in the "4 Channel STS-3 to STS-12" Mode

Q5:2: If the XRT94L43 device is configured to operate in the "4-Channel STS-3 to STS-12 Mapper" Mode, can it be configured to support STS-3c signals?

A5.2: Yes, the exact procedure that one must use to configure the XRT94L43 device to operate in this mode, depends upon whether the user is operating the STS-3 Telecom Bus Interface in the "Rephase ON" or "Rephase OFF" modes, as described below.

IF THE USER IS OPERATING THE STS-3 TELECOM BUS INTERFACE IN THE "REPHASE ON" MODE

If the STS-3 Telecom Bus Interface block is configured to operate in the "Rephase ON" Mode, then the "Transmit SONET POH Processor block" will take on the responsibility of computing the Pointer (e.g., the H1, H2) bytes within the outbound STS-3 signals. As a consequence, the Transmit SONET POH Processor block will (on its own) be able to determine whether or not it is handling an STS-3 or an STS-3c signal (based upon the values of the H1, H2 bytes, corresponding with STS-1 signals # 2 and # 3).

In this case, the user can configure a STS-3 Telecom Bus Interface to support either an STS-3 or STS-3c signal by executing the following steps.

STEP 1 – Set Bits 7 (STS-3 Telecom Bus ON # 3) and 0 (STS-3 REPHASE), within the "Interface Control Register – Byte 3 – STS-3 Telecom Bus 3) to "1" as depicted below.

Interface Control Register – Byte 3 – STS-3 Telecom Bus 3 (Indirect Address = 0x00, 0x38; Direct Address = 0x0138)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 3	STS-3 Telecom Bus Tri-State # 3	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 3	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	1

This step both enables STS-3 Telecom Bus # 3 and also configures it to operate in the "Rephase ON" Mode.

STEP 2 – Set Bits 7 (STS-3 Telecom Bus ON # 2) and 0 (STS-3 REPHASE), within the "Interface Control Register – Byte 2 – STS-3 Telecom Bus 2) to "1" as depicted below.

Interface Control Register – Byte 2 – STS-3 Telecom Bus 2 (Indirect Address = 0x00, 0x39; Direct Address = 0x0139)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 2	STS-3 Telecom Bus Tri-State # 2	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 2	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	1

This step both enables STS-3 Telecom Bus # 2 and also configures it to operate in the "Rephase ON" Mode.

STEP 3 – Set Bits 7 (STS-3 Telecom Bus ON # 1) and 0 (STS-3 REPHASE), within the "Interface Control Register – Byte 1 – STS-3 Telecom Bus 1) to "1" as depicted below.

Interface Control Register – Byte 1 – STS-3 Telecom Bus 1 (Indirect Address = 0x00, 0x3A; Direct Address = 0x013A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 1	STS-3 Telecom Bus Tri-State # 1	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 1	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity ODD	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	1

This step both enables STS-3 Telecom Bus # 1 and also configures it to operate in the "Rephase ON" Mode.

STEP 4 – Bits 7 (STS-3 Telecom Bus ON # 0) and 0 (STS-3 REPHASE), within the "Interface Control Register – Byte 0 – STS-3 Telecom Bus 0) to "1" as depicted below.

Interface Control Register – Byte 0 – STS-3 Telecom Bus 0 (Indirect Address = 0x00, 0x3B; Direct Address = 0x013B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 0	STS-3 Telecom Bus Tri-State # 0	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 0	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	1

This step both enables STS-3 Telecom Bus # 0 and also configures it to operate in the "Rephase ON" Mode.

IF THE USER IS OPERATING THE STS-3 TELECOM BUS INTERFACE IN THE "REPHASE OFF" MODE

If the STS-3 Telecom Bus Interface block is configured to operate in the "Rephase OFF" Mode, then the "Transmit SONET POH Processor block" will NOT take on the responsibility of computing the Pointer (e.g., the H1, H2) bytes within the outbound STS-3 signals. In this mode, the Transmit SONET POH Processor block will determine the location of the SPE or SPEs (within the STS-1 or STS-3c signal) based upon the behavior of the "STSTxA_C1J1_n" input pin (at the Transmit STS-3 Telecom Bus Interface block). As a consequence, the Transmit SONET POH Processor will not (on its own) be able to determine whether or not it is handling an STS-3 or an STS-3c signal (based upon the values of the H1, H2 bytes, corresponding with STS-1 signals # 2 and #3). In this case, the user will have to configure the STS-3 Telecom Bus Interface accordingly.

The user can configure a given STS-3 Telecom Bus Interface to support either an STS-3 or an STS-3c signal. The user can configure the XRT94L43 device to support STS-3c signals (via all four STS-3 Telecom Bus Interfaces) by executing the following steps.

STEP 1a – Set Bits 7 (STS-3 Telecom Bus ON # 3) and 5 (STS-3c REPHASE OFF) to "1" and Bit 0 (STS-3 REPHASE) to "0", within the "Interface Control Register – Byte 3 – STS-3 Telecom Bus 3) to "1" as depicted below.

Interface Control Register – Byte 3 – STS-3 Telecom Bus 3 (Indirect Address = 0x00, 0x38; Direct Address = 0x0138)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 3	STS-3 Telecom Bus Tri-State # 3	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 3	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

This step accomplishes the following.

a. It enables STS-3 Telecom Bus Interface # 3.
b. It configures STS-3 Telecom Bus # 3 to operate in the "Rephase OFF" Mode
c. It configures STS-3 Telecom Bus # 3 to support an STS-3c signal.

STEP 2 – Set Bits 7 (STS-3 Telecom Bus ON # 2) and 5 (STS-3c REPHASE OFF) to "1" and Bit 0 (STS-3 REPHASE) to "0", within the "Interface Control Register – Byte 2 – STS-3 Telecom Bus 2) to "1" as depicted below.

Interface Control Register – Byte 2 – STS-3 Telecom Bus 2 (Indirect Address = 0x00, 0x39; Direct Address = 0x0139)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 2	STS-3 Telecom Bus Tri-State # 2	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 2	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

This step accomplishes the following.

a. It enables STS-3 Telecom Bus Interface # 2.
b. It configures STS-3 Telecom Bus # 2 to operate in the "Rephase OFF" Mode
c. It configures STS-3 Telecom Bus # 2 to support an STS-3c signal.

STEP 3 – Set Bits 7 (STS-3 Telecom Bus ON # 1) and 5 (STS-3c REPHASE OFF) to "1" and Bit 0 (STS-3 REPHASE) to "0", within the "Interface Control Register – Byte 1 – STS-3 Telecom Bus 1) to "1" as depicted below.

Interface Control Register – Byte 1 – STS-3 Telecom Bus 1 (Indirect Address = 0x00, 0x3A; Direct Address = 0x013A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 1	STS-3 Telecom Bus Tri-State # 1	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 1	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity ODD	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

This step accomplishes the following.

a. It enables STS-3 Telecom Bus Interface # 1.
b. It configures STS-3 Telecom Bus # 1 to operate in the "Rephase OFF" Mode
c. It configures STS-3 Telecom Bus # 1 to support an STS-3c signal.

STEP 4 – Set Bits 7 (STS-3 Telecom Bus ON # 0) and 5 (STS-3c REPHASE OFF) to "1" and Bit 0 (STS-3 REPHASE) to "0", within the "Interface Control Register – Byte 0 – STS-3 Telecom Bus 0) to "1" as depicted below.

Interface Control Register – Byte 0 – STS-3 Telecom Bus 0 (Indirect Address = 0x00, 0x3B; Direct Address = 0x013B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-3 Telecom Bus ON # 0	STS-3 Telecom Bus Tri-State # 0	STS-3c REPHASE OFF	STS-3 Telecom Bus Parity Type # 0	STS-3 Telecom Bus J1 ONLY	STS-3 Telecom Bus Parity Odd	STS-3 Telecom Bus Parity Enable	STS-3 REPHASE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

This step accomplishes the following.

a. It enables STS-3 Telecom Bus Interface # 0.
b. It configures STS-3 Telecom Bus # 0 to operate in the "Rephase OFF" Mode
c. It configures STS-3 Telecom Bus # 0 to support an STS-3c signal.

Once the user executes these four steps, then the resulting functional block diagram will be as illustrated below.

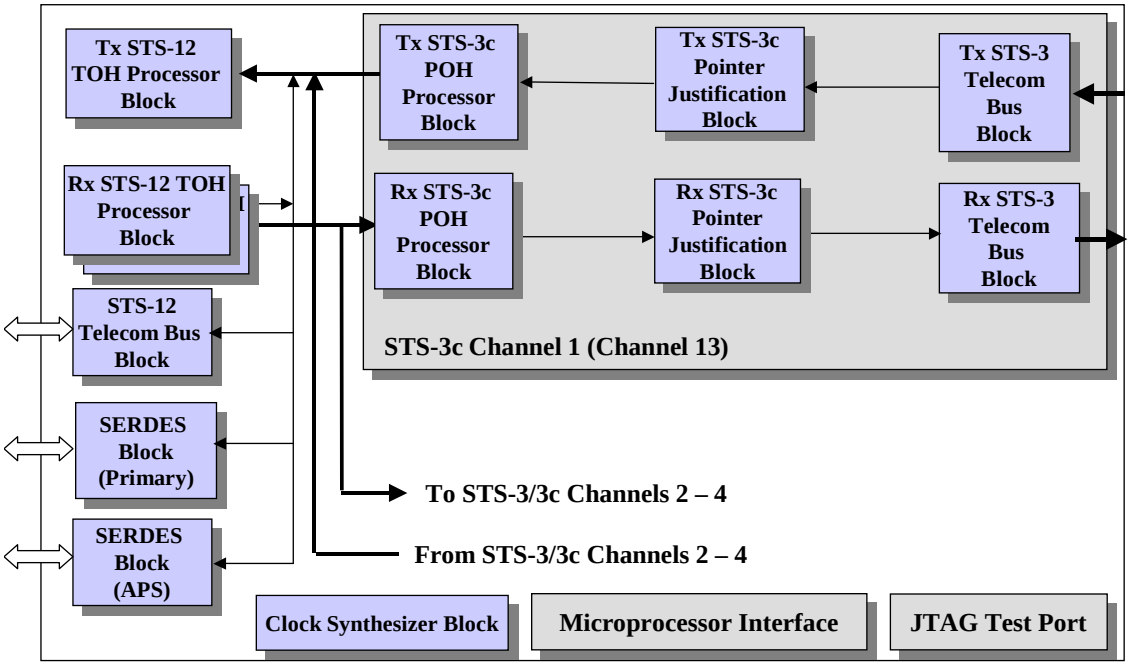

Figure 5-2, Functional Block Diagram of the XRT94L43 device, when it is configured to operate in the "4 Channel STS-3c to STS-12" Mode

Q5.3: Does the XRT94L43 device handle/process STS-3 and STS-3c signals differently.

A5.3: Yes, if the XRT94L43 device is configured to handle STS-3 signals, then its functional block diagram will be as presented below in Figure 5-3.

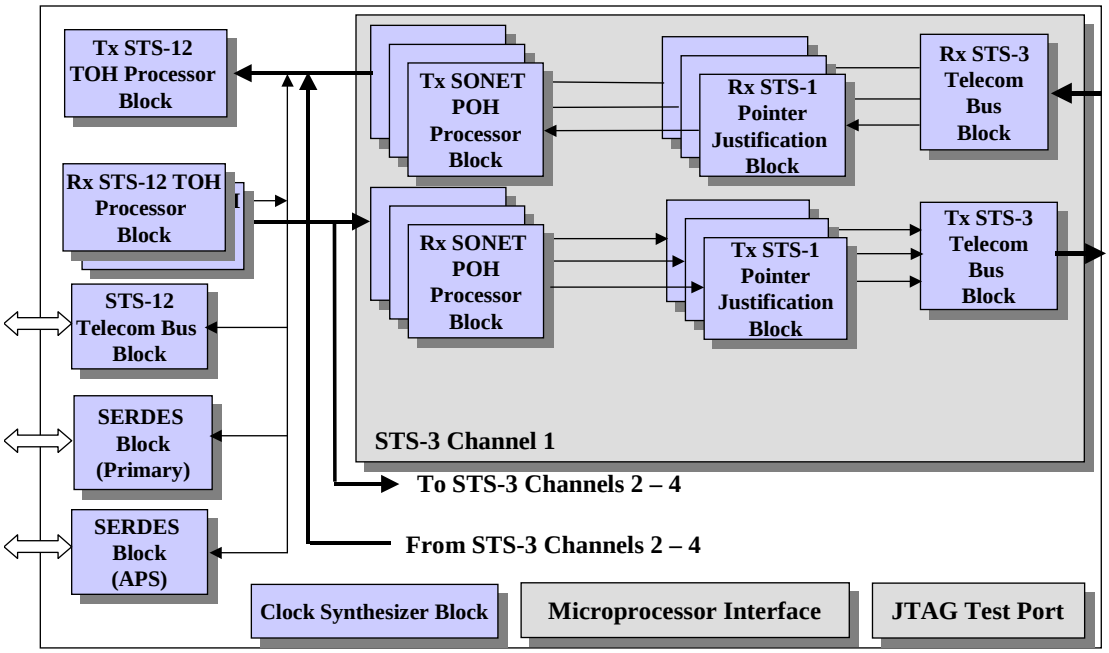

Figure 5-3, Functional Block Diagram of the XRT94L43 device, when it is configured to operate in the "4-Channel STS-3 to STS-12 Mapper" Mode.

Figure 5-3 indicates the following.

In the Receive STS-12 Path:

1. That the Receive STS-12 signal will first pass through the Receive STS-12 TOH Processor block (for TOH Termination and processing); afterwards, this STS-12 signal will be de-interleaved into 12 STS-1 signals.

2. Each of these STS-1 signals will be processed via their corresponding "Receive SONET POH Processor" block (for POH Termination and processing).
3. Afterwards, 3 of these STS-1 signals will be routed to their corresponding "Transmit STS-3 Telecom Bus Block", where they will be output and transmitted to other SONET devices.

NOTE: No POH and TOH insertion (either via software or external input port) will be performed on these STS-1 signals prior to being routed to the Transmit STS-3 Telecom Bus Block.

In the Transmit STS-12 Path:

1. That the incoming STS-3 signal will be received via the "Receive STS-3 Telecom Bus" Block.
2. Afterwards, each STS-1 (within this given STS-3 signal) will be routed to its corresponding Transmit SONET POH Processor block. In this case, POH data can be inserted (either via Software or via External Input port) into these outbound STS-1 SPEs.
3. These STS-1 signals will be byte-interleaved into an STS-12 signal, and then processed by the Transmit STS-12 TOH Processor block. In this case, TOH data can be inserted (either via Software or via External Input port) into this outbound STS-12 signal.

AN ADDITIONAL COMMENT ABOUT OPERATING THE XRT94L43 DEVICE IN THE 4-CHANNEL STS-3 TO STS-12 MODE

If the XRT94L43 device is configured to handle STS-3 (e.g., NOT STS-3c) signals, then these signals will be processed via the exact same Receive SONET POH Processor and Transmit SONET POH Processor blocks (e.g., Channels 1 through 12) which are used when the XRT94L43 device is configured in the "12-Channel DS3/STS-1 to STS-12" Mode.

FOR STS-3c SIGNALS

Now, if the XRT94L43 device is configured to handle STS-3c signals, then its functional block diagram will be as presented below in Figure 5-4.

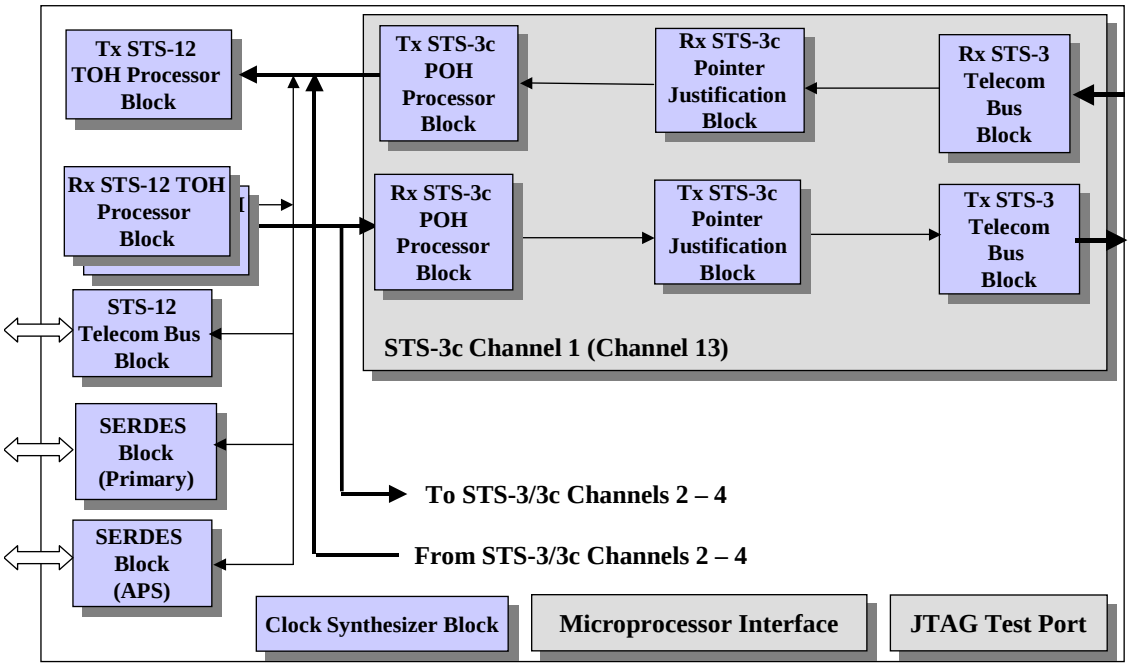

Figure 5-4, Functional Block Diagram of the XRT94L43 device, when it is configured to operate in the "4-Channel STS-3c to STS-12 Mapper" Mode.

Figure 5-4 indicates the following.

In the Receive STS-12 Path:

1. That the Receive STS-12 signal will first pass through the Receive STS-12 TOH Processor block (for TOH Termination and processing); afterwards, this STS-12 signal will be de-interleaved into 4 STS-3c signals.

2. Each of these STS-3c signals will be processed via their corresponding "Receive STS-3c POH Processor" block (for POH Termination and processing).
3. Afterwards, this STS-3c signal will be routed to their corresponding "Transmit STS-3 Telecom Bus Block", where they will be output and transmitted to other SONET devices.

NOTE: No POH and TOH Processing (either via software or external input port) will be performed on these STS-1 signals prior to being routed to the Transmit STS-3 Telecom Bus Block.

In the Transmit STS-12 Path:

1. That the incoming STS-3c signal will be received via the "Receive STS-3c Telecom Bus" Block.
2. Afterwards, the STS-3c signal will be routed to its corresponding Transmit STS-3c POH Processor block. In this case, POH data can be inserted (either via Software or External Input port) into this outbound STS-3c SPE.
3. Each of the four STS-3c signals will be byte-interleaved into an STS-12 signal, and then processed by the Transmit STS-12 TOH Processor block. In this case, TOH data can be inserted (either via Software or via External Input Port) into this outbound STS-12 signal.

AN ADDITIONAL COMMENT ABOUT OPERATING THE XRT94L43 DEVICE IN THE 4-CHANNEL STS-3c TO STS-12 MODE

If the XRT94L43 device is configured to handle STS-3c signals, then these signals will be processed through a different Receive and Transmit POH Processor blocks, from that used in the "12-Channel DS3/STS-1 to STS-12" Mode. In this case, the STS-3c signals will be processed through the Receive STS-3c POH Processor blocks and the Transmit STS-3c POH Processor blocks, which are located in Channels 13 through 16.

Q6: Transmit and Receive SONET POH Processor Block Related Questions

Q6.1: Does the Transmit SONET POH Processor Block contain any "Transmit Path Trace Message" Buffer?

A6.1: Yes, each of the 12 Transmit SONET POH Processor blocks contains a 64 byte "Transmit Path Trace Message" buffer.

The Address Location of each of the 12 Receive Path Trace Message buffers is presented below.

Table 6-1, Address Location of the 12 Transmit Path Trace (J1) Message Buffers

Channel Number	Indirect Address Location	Address Location
0	0x1C, 0x00 – 0x3F	0x1D00 – 0x1D3F
1	0x2C, 0x00 – 0x3F	0x2D00 – 0x2D3F
2	0x3C, 0x00 – 0x3F	0x3D00 – 0x3D3F
3	0x4C, 0x00 – 0x3F	0x4D00 – 0x4D3F
4	0x5C, 0x00 – 0x3F	0x5D00 – 0x5D3F
5	0x6C, 0x00 – 0x3F	0x6D00 – 0x6D3F
6	0x7C, 0x00 – 0x3F	0x7D00 – 0x7D3F
7	0x8C, 0x00 – 0x3F	0x8D00 – 0x8D3F
8	0x9C, 0x00 – 0x3F	0x9D00 – 0x9D3F
9	0xAC, 0x00 – 0x3F	0xAD00 –0xAD3F
10	0xBC, 0x00 – 0x3F	0xBD00 – 0xBD3F
11	0xCC, 0x00 – 0x3F	0xCD00 – 0xCD3F

Q6.2: Does the Receive SONET POH Processor Block contain any "Receive Path Trace Message" Buffer?

A6.2: Yes, each of the 12 Receive SONET POH Processor blocks contains a 64 byte "Receive Path Trace Message" Buffer.

The Address Location of each of the 12 Receive Path Trace Message buffers is presented below.

Table 6-2, Address Location of the 12 Receive Path Trace Message Buffers

Channel Number	Indirect Address Location	Address Location
0	0x14, 0x00 – 0x3F	0x1500 – 0x153F
1	0x24, 0x00 – 0x3F	0x2500 – 0x253F
2	0x34, 0x00 – 0x3F	0x3500 – 0x353F
3	0x44, 0x00 – 0x3F	0x4500 – 0x453F
4	0x54, 0x00 – 0x3F	0x5500 – 0x553F
5	0x64, 0x00 – 0x3F	0x6500 – 0x653F
6	0x74, 0x00 – 0x3F	0x7500 – 0x753F
7	0x84, 0x00 – 0x3F	0x8500 – 0x853F
8	0x94, 0x00 – 0x3F	0x9500 – 0x953F
9	0xA4, 0x00 – 0x3F	0xA500 –0xA53F
10	0xB4, 0x00 – 0x3F	0xB500 – 0xB53F
11	0xC4, 0x00 – 0x3F	0xC500 – 0xC53F

Q6.3: Can the user configure the Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, in the "outbound" STS-1 SPE data-stream (via the outbound STS-12 signal) anytime the corresponding Receive STS-1 TOH Processor block detects certain defect conditions?

A6.3: The user can configure the Transmit SONET POH Processor block to automatically generate and transmit the AIS-P indicator, in the downstream direction (towards the Transmit STS-12 TOH Processor block) anytime the corresponding Receive STS-1 TOH Processor block declares any of the following defect conditions: LOS, LOF, SD, SF and AIS-L. Figure 6-1 presents an illustration of the Transmit SONET POH Processor block transmitting the AIS-P indicator, within its outbound STS-1 signal (via the outbound STS-12 signal) whenever the corresponding Receive STS-1 TOH Processor block detects and declares either the LOS, LOF, SD, SF or AIS-L defect conditions.

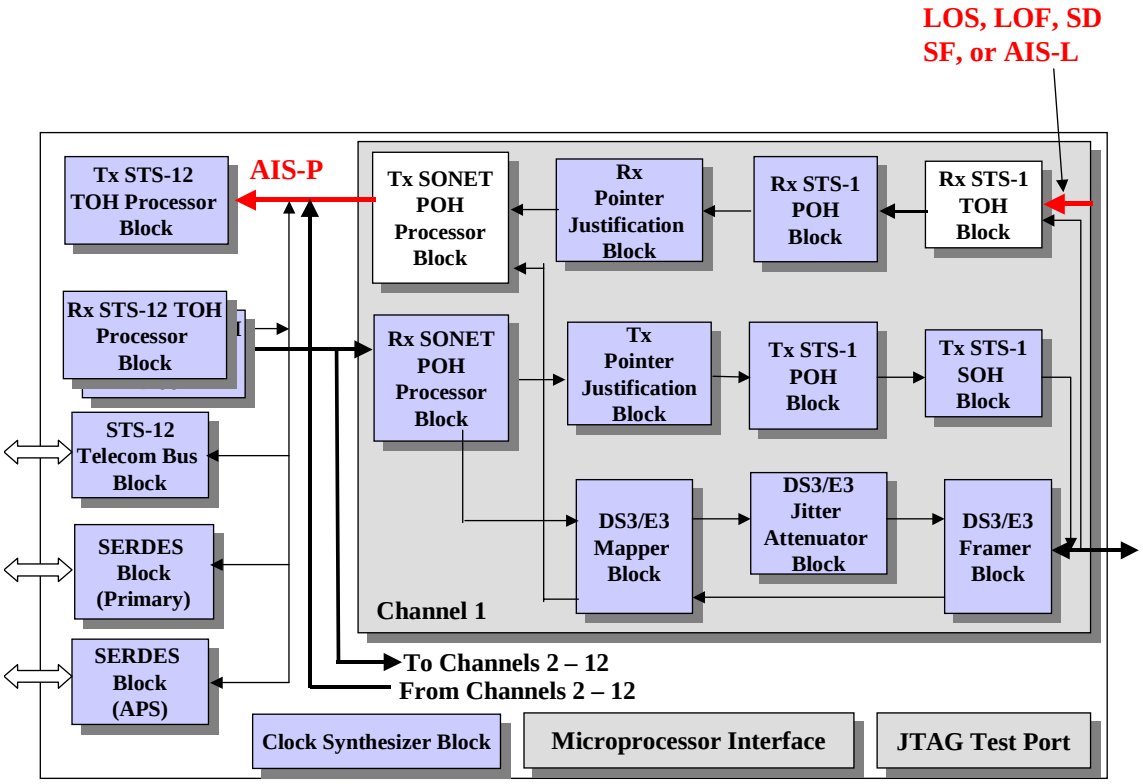

Figure 6-1, Illustration of the Transmit SONET POH Processor block automatically transmitting AIS-P downstream, whenever the corresponding Receive STS-1 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions.

Configuring this Automatic AIS-P Generation

The user can configure the Transmit SONET POH Processor block to automatically generate and transmit the AIS-P indicator, via its outbound STS-1 signal (via the outbound STS-12 signal) whenever (and for the duration that) the corresponding Recevie STS-1 TOH Processor block declares either the LOS, LOF, AIS-L, SD or SF defect condition, by executing the following step.

STEP 1 – Set Bits 0 (Transmit AIS-P – via Downstream STS-1s – Enable), 2 (Transmit AIS-P upon SF), 3 (Transmit AIS-P upon SD), 4 (Transmit AIS-P upon LOF), and 5 (Transmit AIS-P upon LOS) to "1" as depicted below.

Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register (Indirect Address = 0xN2, 0x6B; Direct Address = 0xN36B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Transmit AIS-P (via Downstream STS-1s) upon LOS	Transmit AIS-P (via Downstream STS-1s) upon LOF	Transmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	Unused	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/W
0	0	1	1	1	1	0	1

Q6.4: Does the XRT94L43 device permit the user to control the values of certain POH bytes, within the 12 outbound STS-1 signals (that are ultimately mapped into an STS-12 signal), via on-chip registers?

A6.4: Yes, the circuitry associated with each of the 12 Transmit SONET POH Processor blocks (within the XRT94L43 device) permits the user to control all of the following POH bytes via on-chip registers.

- J1
- C2
- G1
- F2
- H4
- Z3
- Z4
- Z5

The on-chip registers associated with each of these POH bytes are presented below.

For the J1 Byte:

Transmit SONET Path – Transmitter J1 Byte Value Register (Indirect Address = 0xN8, 0x93; Direct Address = 0xN993)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_J1_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The Transmit SONET Path – Transmitter J1 Byte Value Register should only be used if the user has selected a “Path Trace Message” size of 1 byte.

For the C2 Byte:

Transmit SONET Path – Transmit C2 Byte Value Register (Indirect Address = 0xN8, 0x9B; Direct Address = 0xN99B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the G1 Byte:

Transmit SONET Path – Transmit G1 Byte Value Register (Indirect Address = 0xN8, 0x9F; Direct Address = 0xN99F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the F2 Byte:

Transmit SONET Path – Transmit F2 Byte Value Register (Indirect Address = 0xN8, 0xA3; Direct Address = 0xN9A3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the H4 Byte:

Transmit SONET Path – Transmit H4 Byte Value Register (Indirect Address = 0xN8, 0xA7; Direct Address = 0xN9A7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the Z3 Byte:

Transmit SONET Path – Transmit Z3 Byte Value Register (Indirect Address = 0xN8, 0xAB; Direct Address = 0xN9AB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the Z4 Byte:

Transmit SONET Path – Transmit Z4 Byte Value Register (Indirect Address = 0xN8, 0xAF; Direct Address = 0xN9AF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the Z5 Byte:

Transmit STS-1 Path – Transmit Z5 Byte Value Register (Indirect Address = 0xN8, 0xB3; Direct Address = 0xN9B3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Q6.5: Does the XRT94L43 device permit the user to monitor the values of certain POH bytes by software (via on-chip registers), within the 12 inbound STS-1 signals that have been de-mapped from STS-12?

A6.5: Yes, the circuitry associated with each of the 12 Receive SONET POH Processor blocks (within the XRT94L43 device) permits the user to monitor the values of all of the POH bytes (within each of the incoming STS-1 signals) that have been de-mapped from STS-12; via on-chip registers.

The on-chip registers associated with each of these POH bytes are presented below.

For the J1 Byte:

Receive SONET Path – Receive J1 Byte Capture Register (Indirect Address = 0xN0, 0xD3; Direct Address = 0xN1D3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the B3 Byte:

Receive SONET Path – Receive B3 Byte Capture Register (Indirect Address = 0xN0, 0xD7; Direct Address = 0xN1D7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the C2 Byte:

Receive SONET Path – Receive C2 Byte Capture Register (Indirect Address = 0xN0, 0xDB; Direct Address = 0xN1DB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the G1 Byte:

Receive SONET Path – Receive G1 Byte Capture Register (Indirect Address = 0xN0, 0xDF; Direct Address = 0xN1DF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the F2 Byte:

Receive SONET Path – Receive F2 Byte Capture Register (Indirect Address = 0xN0, 0xE3; Direct Address =0xN1E3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the H4 Byte:

Receive SONET Path – Receive H4 Byte Capture Register (Indirect Address = 0xN0, 0xE7; Direct Address = 0xN1E7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the Z3 Byte:

Receive SONET Path – Receive Z3 Byte Capture Register (Indirect Address = 0xN0, 0xEB; Direct Address = 0xN1EB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the Z4 Byte:

Receive SONET Path – Receive Z4 (K3) Byte Capture Register (Indirect Address = 0xN0, 0xEF; Direct Address = 0xN1EF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the Z5 Byte:

Receive SONET Path – Receive Z5 Byte Capture Register (Indirect Address = 0xN0, 0xF3; Direct Address = 0xN1F3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Q6.6: Does the XRT94L43 device permit one to arbitrarily fix the Pointer Values of each STS-1/VC-3 within the outbound STS-12 data-stream?

A6.6: If one has configured the XRT94L43 device to map 12 DS3 signals into an STS-12, then one can assigned the offsets (of the STS-1 SPEs with respect to the STS-12 frame boundary) to ANY Valid pointer value. Further, these "user-configured" pointer values (and the corresponding STS-1 SPE to STS-12 Frame Boundary offsets) will remain in affect until changed again by the user.

Example:

For example, the user can set each of the 12 Pointer values to 522 (or 0x020A) by executing the following steps for each of the 12 Channels.

STEP 1 – Set the value of the H1 Byte the outbound STS-12 data-stream

In this case, we need to set the "H1 Byte" to the value of 0x9A". This is accomplished by writing the value 0x9A into the "Transmit SONET Path – Transmit Arbitrary H1 Pointer Register (Address = 0xN9BF), as depicted below.

Transmit SONET Path – Transmit Arbitrary H1 Pointer Register (Indirect Address = 0xN8, 0xBF; Direct Address = 0xN9BF, where N ranges in value from 0x01 to 0x0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NDF Bits				SS Bits		H1 Pointer Value[9:8]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	1	1	0	1	0

STEP 2 – Set the value of the H2 Byte without the outbound STS-12 data-stream

In this case, we need to set the "H2 Byte" to the value of "0x0A". This is accomplished by writing the value "0x0A" into the "Transmit SONET Path – Transmit Arbitrary H2 Pointer Register (Address = 0 xN9C3, as depicted below.

Transmit SONET Path – Transmit Arbitrary H2 Pointer Register (Indirect Address = 0xN8, 0xC3; Direct Address = 0xN9C3; where N ranges in value from 0x01 to 0x0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	1	0

STEP 3- Command the Transmit SONET POH Processor block (within Channel N) to start using these (above-specified) values for the H1/H2 Bytes.
The user can accomplish this by setting Bit 5 (Pointer Force), within the "Transmit SONET Path – Transmit Path Control Register (Address = 0xN9B7), to "1" as depicted below.

Transmit SONET Path – Transmit Path Control Register (Indirect Address = 0xN8, 0xB7; Direct Address = 0xN9B7; where N ranges in value from 0x01 to 0x0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0 -> 1	1	0	0	0	0

NOTES:
1. This approach will NOT for those channels in which the XRT94L43 device is handling STS-1 data.
2. After the user has set the "Pointer Force" bit-field to "1", the XRT94L43 device will (internally) go back and RESET the "Pointer Force" bit-field to "0". The user does not need to go back and manually reset this bit-field to "0".

Q7: STS-12/STM-4 Telecom Bus Related Questions

Q7.1: What signals exist within the Transmit STS-12/STM-4 Telecom Bus Interface block?

A7.1: The Transmit STS-12/STM-4 Telecom Bus Interface consists of the following signals.

- TxA_D[7:0] – The Transmit STS-12/STM-4 Telecom Bus – Data Output pins
- TxA_CLK – The Transmit STS-12/STM-4 Telecom Bus – Clock Output pin
- TxA_PL – The Transmit STS-12/STM-4 Telecom Bus – Payload (or SPE) Data Indicator output pin
- TxA_C1J1 – The Transmit STS-12/STM-4 Telecom Bus – C1 and J1 Byte Indicator output pin
- TxA_DP – The Transmit STS-12/STM-4 Telecom Bus – Data Parity Output pin
- TxA_ALARM – The Transmit STS-12/STM-4 Telecom Bus – Alarm Indicator Output pin
- TxSBFP – The Transmit STS-12/STM-4 Telecom Bus Framing Alignment Input pin.

The functional description of each of these pins is summarized in the table below.

Table 7-1, Pin Description of the Transmit STS-12/STM-4 Telecom Bus Interface

Pin Name	Pin Number	Type	Description
TxA_CLK	G2	O	**Transmit STS-12/STM-4 Telecom Bus Clock Signal:** This output clock signal functions as the clock source for the Transmit STS-12/STM-4 Telecom Bus. All signals (which are output via the Transmit STS-12/STM-4 Telecom Bus Interface) are updated upon the rising edge of this clock signal. This clock signal operates at 77.76MHz and is derived from the Clock Synthesizer block
TxA_D0 TxA_D1 TxA_D2 TxA_D3 TxA_D4 TxA_D5 TxA_D6 TxA_D7	G1 J5 J2 H5 E1 F2 F1 E3	O	**Transmit STS-12/STM-4 Telecom Bus Interface – Data Bus Output pins:** These 8 output pins function as the "Transmit STS-12/STM-4 Telecom Bus" output data bus. If the STS-12/STM-4 Telecom Bus Interface is enabled, then all "outbound" STS-12/STM-4 data will be output (in a byte-wide manner) via these output pins upon the rising edge of the "TxA_CLK" output.

Table 7-1, Pin Description of the Transmit STS-12/STM-4 Telecom Bus Interface (Continued)

Pin Name	Pin Number	Type	Description
TxA_C1J1	J1	O	**The Transmit STS-12/STM-4 Telecom Bus – C1 and J1 Byte Indicator Output pin** The exact behavior of this output pin depends upon whether the Transmit STS-12/STM-4 Telecom Bus Interface has been configured to operate in the "C1J1" Mode or in the "J1 Only" Mode, as described below. **In the "C1J1" Mode** This output pin will pulse "high" coincident to any of the following events. • Whenever the very first C1 (J0) byte of a given outbound STS-12/STM-4 frame is being output via the "TxA_D[7:0]" output pins. • Whenever a J1 byte (corresponding to any of the 12 STS-1s within this outbound STS-12 signal) is being output via the "TxA_D[7:0]" output. This output pin will be "low" during all other times. **NOTES:** 1. In this mode, this output pin will pulse "high" thirteen (13) times for each "outbound" STS-12 frame. 2. In this mode, the "C1" byte will be uniquely designated by being the only pulse (in this output pin) that occurs coincident to the "TxA_PL" output pin being "low". For each of the remaining 12 times that this output pin pulse "high", the "TxA_PL" output pin will be "high". 3. In this mode, the "offset" between each of the 12 SPEs and the TOH can be determined by the amount of time (in terms of "TxA_CLK" clock period) that elapses between the occurrence of the "C1 byte" pulse and that of the "J1 byte" pulses. **In the "J1 Only" Mode** This output pin will pulse "high" coincident to whenever a J1 byte (corresponding to any of the 12 STS-1s within this outbound STS-12 signal) is being output via the "TxA_D[7:0]" output. This output pin will be "low" during all other times.

Table 7-1, Pin Description of the Transmit STS-12/STM-4 Telecom Bus Interface (Continued)

Pin Name	Pin Number	Type	Description
TxA_DP	H1	O	**The Transmit STS-12/STM-4 Telecom Bus – Data Parity Output pin** The Transmit STS-12/STM-4 Telecom Bus Interface block can be configured to compute either the even or odd parity of either of the following sets of data. a. The data being output via the "TxA_D[7:0]" output pins, or b. The data being output via the "TxA_D[7:0]" output pins, and the current state of the "TxA_C1J1" and "TxA_PL" output signals. Depending upon the user's configuration, the Transmit STS-12/STM-4 Telecom Bus Interface block will compute the parity (over the above-mentioned set of signals) and will output this parity value (via this output pin) coincident to when the corresponding data/signals are being output via the "TxA_D[7:0]", TxA_C1J1 and "TxA_PL" output pins.
TxA_ALARM	J3	O	**The Transmit STS-12/STM-4 Telecom Bus – Alarm Indicator Output pin** The purpose of this output pin is to indicate whenever a given STS-1 (within the outbound STS-12 signal) is transporting the AIS-P indicator. This output pin will pulse "high" coincident to whenever a byte corresponding to the "alarmed" STS-1 signal, is being output via the "TxA_D[7:0]" output pin. Conversely, this output pin will toggle and remain "low" whenever the Transmit STS-12/STM-4 Telecom Bus Interface outputs a byte (via the "TxA_D[7:0]" output pins; that corresponds to an STS-1 that is not carrying the AIS-P indicator.

Table 7-1, Pin Description of the Transmit STS-12/STM-4 Telecom Bus Interface (Continued)

Pin Name	Pin Number	Type	Description
TxSBFP	K5	I	**The Transmit STS-12/STM-4 Telecom Bus – Framing Alignment Input pin** The user has the option to configure the Transmit STS-12/STM-4 Telecom Bus Interface block to align its transmission of STS-12/STM-4 frames to an 8kHz signal that is applied to this input pin. If the user wishes to use this feature then he/she should apply a pulse (which is one "TxA_CLK" period in width) to this input pin. By default, the Transmit STS-12/STM-4 Telecom Bus Interface will transmit the very first byte of a given STS-12/STM-4 frame, coincident with the pulse at this input pin. **NOTE:** The XRT94L43 device also permits the user to specify a delay (in terms of TxA_CLK cycles) between a pulse at this input pin, and the instant that the first byte of a given STS-12/STM-4 frame is output via the "TxA_D[7:0]" output pins. This "delay" is programmed via on-chip registers.

Q7.2: What signals exist within the Receive STS-12/STM-4 Telecom Bus Interface block?

A7.2: The Receive STS-12/STM-4 Telecom Bus Interface consists of the following signals.

- RxD_D[7:0] – The Receive STS-12/STM-4 Telecom Bus – Data Input pins
- RxD_CLK – The Receive STS-12/STM-4 Telecom Bus – Clock Input pin
- RxD_PL – The Receive STS-12/STM-4 Telecom Bus – Payload (or SPE) Data Indicator input pin
- RxD_C1J1 – The Receive STS-12/STM-4 Telecom Bus – C1 and J1 Byte Indicator Input pin
- RxD_DP – The Receive STS-12/STM-4 Telecom Bus – Data Parity Input pin
- RxD_ALARM – The Receive STS-12/STM-4 Telecom Bus – Alarm Indicator Input pin

The functional description of each of these pins is summarized in the table below.

Table 7-2, Pin Description of the Receive STS-12/STM-4 Telecom Bus Interface

Pin Name	Pin Number	Type	Description
RxD_D0 RxD_D1 RxD_D2 RxD_D3 RxD_D4 RxD_D5 RxD_D6 RxD_D7	U3 V3 U2 T1 V5 U1 W1 V1	I	**The Receive STS-12/STM-4 Telecom Bus Data Input pins** All inbound STS-12/STM-4 data will be accepted via these input pins, in a byte-wide manner. Data on these pins will be sampled upon the rising edge of "RxD_CLK". The MSB (Most Significant Bit) will be accepted via the "RxD_D7" input pin, and the LSB (Least Significant Bit) will be input via the "RxD_D0" input pin.
RxD_CLK	V4	I	**The Receive STS-12/STM-4 Telecom Bus – Clock Input Pin** This pin receives a 77.76MHz clock signal. The Receive STS-12/STM-4 Telecom Bus Interface will use the rising edge of this signal to sample and latch the data, residing on the "RxD_D[7:0]" input pins. Additionally, the Receive STS-12/STM-4 Telecom Bus Interface will also use the rising edge of this clock signal to sample and latch the "RxD_PL", "RxD_C1J1", RxD_DP, and "RxD_ALARM" input pins. **NOTE:** This input clock signal will also function as the timing source for the "Receive STS-12 TOH Processor block" and the "Receive SONET POH Processor block".
RxD_PL	U5	I	**The Receive STS-12/STM-4 Telecom Bus – Payload Data Indicator Input pin** The Receive STS-12/STM-4 Telecom Bus Interface can use this input pin in order to determine whether or not it currently reading in SPE data via the "RxD_D[7:0]" output pins. This input pin will be "high" coincident to whenever SPE data is being input via the "RxD_D[7:0]" input pins. Conversely, this data will be "low" coincident to whenever non-SPE data is being input via the "RxD_D[7:0]" input pins. This input pin is sampled upon the rising edge of "RxD_CLK". **NOTE:** This input pin is only active if the STS-12/STM-4 Telecom Bus Interface has been configured to operate in the "Re-Phase OFF" Mode.

Table 7-2, Pin Description of the Receive STS-12/STM-4 Telecom Bus Interface (Continued)

Pin Name	Pin Number	Type	Description
RxD_C1J1	V2	I	**The Receive STS-12/STM-4 Telecom Bus – C1 and J1 Byte Indicator Input pin** The exact behavior of this input pin depends upon whether the Transmit STS-12/STM-4 Telecom Bus Interface has been configured to operate in the "C1J1" Mode or in the "J1 Only" Mode, as described below. **In the "C1J1" Mode** This input pin will be pulsed "high" coincident to any of the following events. • Whenever the very first C1 (J0) byte of a given outbound STS-12/STM-4 frame is being input via the "RxD_D[7:0]" input pins. • Whenever a J1 byte (corresponding to any of the 12 STS-1s within this inbound STS-12 signal) is being input via the "RxD_D[7:0]" input. This input pin will be "low" during all other times. **NOTES:** 1. In this mode, this input pin will be pulsed "high" thirteen (13) times for each "inbound" STS-12 frame. 2. In this mode, the "C1" byte will be uniquely designated by being the only pulse (in this input pin) that occurs coincident to the "RxD_PL" input pin being "low". For each of the remaining 12 times that this input pin pulses "high", the "RxD_PL" input pin will be "high". 3. In this mode, the "offset" between each of the 12 SPEs and the TOH can be determined by the amount of time (in terms of RxD_CLK clock periods) that elapses between the occurrence of the "C1 byte" pulse and that of the "J1 byte" pulses. **In the "J1 Only" Mode** This input pin will be pulsed "high" coincident to whenever a J1 byte (corresponding to any of the SPEs within this inbound STS-12 signal) is being input via the "RxD_D[7:0]" input . This input pin should be "low" during all other times. **NOTE:** This input pin is only active if the STS-12/STM-4 Telecom Bus Interface has been configured to operate in the "Re-Phase OFF" Mode.

Table 7-2, Pin Description of the Receive STS-12/STM-4 Telecom Bus Interface (Continued)

Pin Name	Pin Number	Type	Description
RxD_DP	U4	I	**The Receive STS-12/STM-4 Telecom Bus – Data Parity Input pin** The Receive STS-12/STM-4 Telecom Bus Interface block can be configured to compute and verify either the even or odd parity of either of the following sets of data. a. The data being receive via the "RxD_D[7:0]" input pins, or b. The data being received via the "RxD_D[7:0]" input pins, and the current state of the "RxD_C1J1", and the "RxD_PL" input signals. Depending upon the user's configuration, the Receive STS-12/STM-4 Telecom Bus Interface block will some parity bits via the "RxD_DP" input pin. The Receive STS-12/STM-4 Telecom Bus Interface block will then compute and verify these parity bits based upon the data that it receives via the "RxD_D[7:0]", "RxD_PL" and "RxD_C1J1" input pins.
RxD_ALARM	T2	I	**The Receive STS-12/STM-4 Telecom Bus - Alarm Indicator Input pin** The purpose of this input pin is to indicate whenever a given STS-1/STS-3c signal (within the inbound STS-12 signal) is declaring an AIS-P condition. This input pin will be pulsed "high" coincident to whenever a byte corresponding to the "alarmed" STS-1/STS-3c signal is being received via the "RxD_D[7:0]" input pin. **NOTE:** If the Receive STS-12/STM-4 Telecom Bus Interface block samples this input pin "high", then the Receive SONET POH Processor block (that corresponds with the alarmed inbound STS-1/STS-3c signal) will automatically declare the AIS-P condition. This Receive SONET POH Processor block will continue to declare the AIS-P condition for the duration that the Receive STS-12/STM-4 Telecom Bus Interface block continues to sample this input pin "high". **NOTE:** This input pin is only active if the STS-12/STM-4 Telecom Bus Interface has been configured to operate in the "Re-Phase OFF" Mode.

Q7.3: Can the user configure the Transmit STS-12/STM-4 Telecom Bus Interface block to align its transmit of an STS-12 or STM-4 frame, with an external 8kHz signal?

A7.3: The answer to this question is "Yes". The Transmit STS-12/STM-4 Telecom Bus can be configured to align its transmission of outbound STS-12/STM-4 frames with an 8kHz pulse that is applied to the "TxSBFP" input pin.

Ordinarily, the Transmit STS-12/STM-4 Telecom Bus will align its transmission of STS-12/STM-4 frames such that it will transmit the very first byte of a given STS-12/STM-4 frame during the same "TxA_CLK" period that the "TxSBFP" input pin is "pulsed" high. However, if desired, the user can configure the Transmit STS-12/STM-4 Telecom Bus Interface block to transmit the very first byte of an "outbound" STS-12/STM-4 frame, a few "TxA_CLK" periods AFTER "TxSBFP" has been pulsed "high".

This can be achieved by writing the appropriate value into the "STS-12/STM-4 Telecom Bus Control Register – Byte 3 and Byte 2" as depicted below.

STS-12/STM-4 Telecom Bus Control Register – Byte 3 (Indirect Address = 0x00, 0x34; Direct Address = 0x0134)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HRSYNC_Delay[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STS-12/STM-4 Telecom Bus Control Register – Byte 2 (Indirect Address = 0x00, 0x35; Direct Address = 0x0135)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HRSYNC_Delay[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

These two registers present a "16-bit" Latency Register. The "STS-12/STM-4 Telecom Bus Control Register – Byte 3" is the "Upper Byte" Register, and the "STS-12/STM-4 Telecom Bus Control Register – Byte 2" is the "Lower Byte" Register.

If the user writes the value "0x0001" into this register, then the Transmit STS-12/STM-4 Telecom Bus Interface block will be configured to transmit the very first byte of a given "outbound" STS-12/STM-4 frame, one "TxA_CLK" period, after the "TxSBFP" input pin has been pulsed "high" by the 8kHz signal. If the user writes the value "0x0002" into

this register, then the Transmit STS-12/STM-4 Telecom Bus Interface block will be configured to transmit the very first byte of a given "outbound" STS-12/STM-4 frame, two "TxA_CLK" periods after the "TxSBFP" input pin has been pulsed "high" by the 8kHz signal, and so on.

NOTE: The user can also employ this "alignment" of outbound STS-12/STM-4 frames (with respect to the 8kHz pulses at the TxSBFP input pin) as well as the use of the above-mentioned "Delay" registers, if the XRT94L43 device has been configured to operate in the "STS-12/STM-4 PECL Interface" Mode. For more details on this feature, please see Question Q13.3.

Q8: DS3/E3 Framer Block Related Questions

Q8.1: What sub-blocks exist within the DS3/E3 Framer block (within each channel of the XRT94L43 device)?

A8.1: Each of the 12 DS3/E3 Framer blocks consist of the following functional blocks.

- The DS3/E3 Frame Generator block
- The Primary DS3/E3 Frame Synchronizer block
- The Secondary DS3/E3 Frame Synchronizer block

The role/purpose that each of these functional block play is presented below.

The DS3/E3 Frame Generator Block

The purpose of the DS3/E3 Frame Generator block is to accept a data-stream (via the System-side Interface) and to map this data into the payload bits within an "outbound" DS3 or E3 data-stream. This resulting DS3 or E3 data-stream is output via the "Line-Side" Interface.

The function of the DS3/E3 Frame Generator block is identical to that of the "Transmit DS3/E3 Framer" block that is described for Exar's XRT72L5X and XRT74L7X Family of DS3/E3 Framer Products.

In addition to mapping data into a DS3 or E3 data-stream, the DS3/E3 Frame Generator block is also capable of supporting the following functions.

- To (optionally) encode the "outbound" DS3 or E3 data-stream into the B3ZS or HDB3 line code.
- To source and transmit LAPD/PMDL messages
- To transmit FEAC (Far-End Alarm & Control) Messages – DS3 C-Bit Parity Applications only.
- To transmit TTB (Trail Trace Buffer) Messages – E3, ITU-T G.832 Applications only.
- To transmit the FERF (Far-End Receive Failure) and FEBE (Far-End Block Error)
- To transmit the AIS (Alarm Indication Signal) Pattern upon software command.

NOTE: The DS3/E3 Frame Generator block can also be configured to automatically transmit the AIS condition, anytime (and for the duration) that the Secondary DS3/E3 Frame Synchronizer block is declaring either the "LOS", "LOF", or AIS condition.

- To transmit the DS3 Idle Pattern upon software command (DS3 C-bit Parity Applications only).

The Primary DS3/E3 Frame Synchronizer block

The purpose of the Primary DS3/E3 Frame Synchronizer block is to receive a DS3 or E3 data-stream (from some other entity) and to perform the following functions.

- To (optionally) decode the "inbound" DS3 or E3 data-stream from the B3ZS or HDB3 line code.
- To acquire and maintain frame synchronization with the incoming DS3 or E3 data-stream.
- To receive (and terminate) LAPD/PMDL Messages
- To receive FEAC Messages (DS3, C-bit Parity applications only)
- To receive TTB Messages (E3, ITU-T G.832 applications only)
- To detect and declare the LOS (Loss of Signal), OOF (Out of Frame), AIS or FERF defects.
- To detect and increment Performance Monitor registers in response to any of the following events.
    a. Line Code Violations
    b. Excessive Zeros
    c. Framing Bit/Byte Errors
    d. P-Bit Errors (DS3 Applications)
    e. CP-Bit Errors (DS3 Applications)
    f. BIP-8 Errors (E3, ITU-T G.832 Applications)
    g. BIP-4 Errors (E3, ITU-T G.751 Applications)
    h. FEBE Events

The function of the Primary DS3/E3 Frame Synchronizer block is identical to that of the "Receive DS3/E3 Framer" block that is described for Exar's XRT72L5X and XRT74L7X Family of DS3/E3 Framer Products.

The Secondary DS3/E3 Frame Synchronizer block

The main (and original) purpose of the Secondary DS3/E3 Frame Synchronizer block was to permit the user to easily route DS3/E3 data to the System-side interface of the Frame Generator block. As framed DS3 or E3 data is routed through either of these "DS3/E3 Frame Synchronizer" blocks, the "Secondary DS3/E3 Frame Synchronizer block will identify the locations of the overhead bits/bytes (within this DS3 or E3 data-stream) and will convey this information to the "DS3/E3 Frame Generator" block.

NOTE: In addition to this basic function of "easing the process" of routing DS3/E3 data through the DS3/E3 Frame Generator block, the Secondary DS3/E3 Frame Synchronizer is also capable of performing the following operations.

- Detecting and declaring the LOS Defect
- Detecting and declaring the AIS Defect
- Detecting and declaring the LOF/OOF Defect
- Detecting and declaring the DS3 Idle Condition

Q8.2: What framing formats are supported by the DS3/E3 Framer blocks?

A8.2: The DS3/E3 Framer blocks (within the XRT94L43 device) can be configured to support the following framing formats.

- DS3, M13 (aka M23) Framing Format
- DS3, C-bit Parity Framing Format
- E3, ITU-T G.751 Framing Format
- E3, ITU-T G.832 Framing Format

NOTE: The DS3/E3 Framer block can be configured to support either the pre October 1998 or the post October 1998 version of the E3, ITU-T G.832 framing format.

Q8.3: What are the differences between the Primary and Secondary Frame Synchronizer blocks?

A8.3: The Primary Frame Synchronizer block is capable of performing all of the following functions over and above that which the Secondary Frame Synchronizer block can perform.

- Reception of FEAC Messages (for DS3, C-bit Parity Applications only)
- Reception of LAPD/PMDL Messages (for DS3, C-bit Parity Applications only)
- To detect and flag P-bit, CP-bit and Framing Bit (F and M-bit) errors (for DS3 applications only)
- To detect and flag BIP-8 and Framing Alignment byte errors (for E3, ITU-T G.832 applications only)
- To detect and flag Line Code Violations (LCVs) and Excessive Zeros (EXZs).

Q8.4: Which Frame Generator/Frame Synchronizer Configurations are recommended for handling normal DS3/E3 traffic?

A8.4: There are two Frame Generator/Frame Synchronizer configurations that are used quite often. These two configurations are referred to (in the XRT94L43 Data Sheet) as Frame Generator/Frame Synchronizer Configuration Numbers # 23 and # 28. Each of these Frame Generator/Frame Synchronizer Configurations is described below.

1. Frame Generator/Frame Synchronizer Configuration # 23

In "Frame Generator/Frame Synchronizer Configuration # 23" the Primary DS3/E3 Frame Synchronizer block operates in the Egress Path. Additionally, the Secondary DS3/E3 Frame Synchronizer and DS3/E3 Frame Generator blocks will be operating in the Ingress Path. An illustration of "Frame Generator/Frame Synchronizer Configuration # 23" is presented below in Figure 8-1.

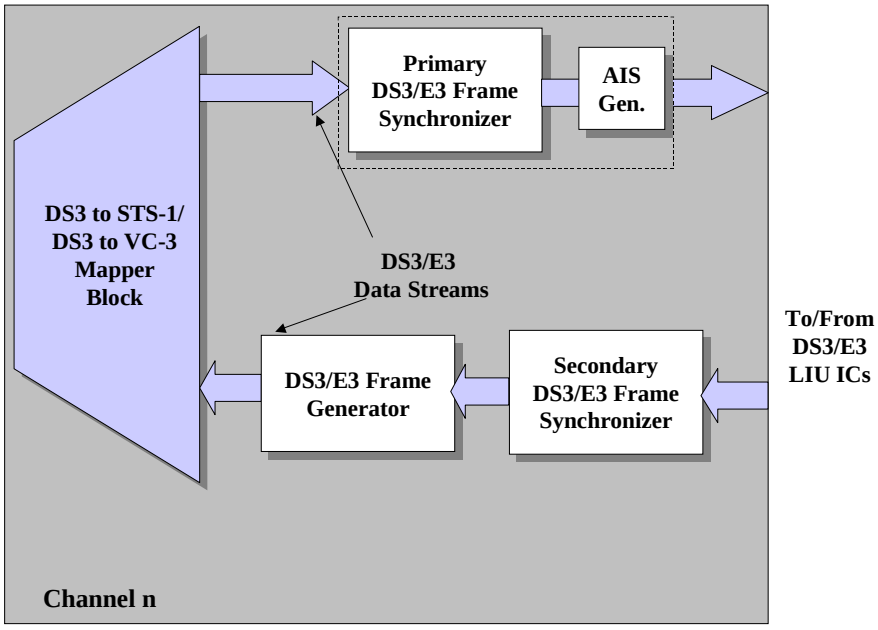

Figure 8-1, Illustration of Frame Generator/Frame Synchronizer Configuration # 23

Frequently Asked Questions regarding the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/STM-4 Mapper IC

Preliminary

August 15, 2006

How to Configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer Configuration # 23

The user can configure the DS3/E3 Frame Generator/Frame Synchronizer blocks (within a particular channel) to operate in this orientation by executing the following steps.

STEP 1 – Write the value "0xC0" into the "Mapper Control" register, as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control" Register ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

This particular step configures the DS3/E3 Framer block (within the corresponding Channel) to operate in Frame Generator/Frame Synchronizer Configuration # 28.

STEP 2 – Invert the Clock (with respect to the DS3 Data) that is being generated by the Frame Generator Block.

This is accomplished by setting Bit 2 (DS3/E3 CLK OUT Invert) to "1" as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3 CLK OUT Invert	DS3/E3 CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	1	0	0

NOTE: This step is necessary if one intend to configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer Configuration # 23". This step will provide the Mapper Block will sufficient set-up and hold time with the DS3/E3 Data being generated by the Frame Generator block.

2. Frame Generator/Frame Synchronizer Configuration # 28

In "Frame Generator/Frame Synchronizer" Configuration # 28, the "Primary DS3/E3 Frame Synchronizer block operates in the Ingress Path. Additionally, the Secondary DS3/E3 Frame Synchronizer and DS3/E3 Frame Generator blocks will be operating in the Egress Path. An illustration of "Frame Generator/Frame Synchronizer Configuration # 28" is presented below in Figure 8-2.

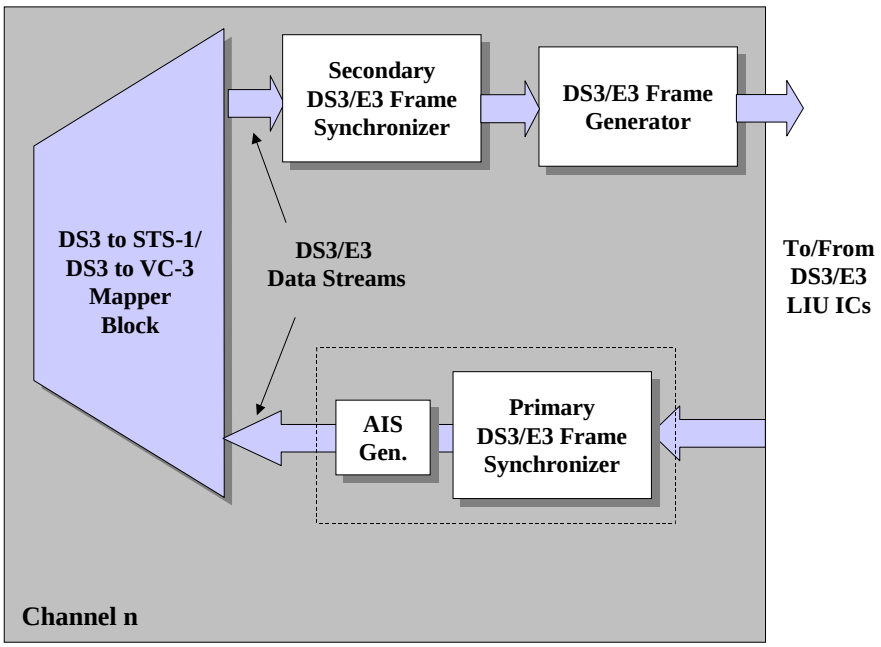

Figure 8-2, Illustration of Frame Generator/Frame Synchronizer Configuration # 28

How to Configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer Configuration # 28

The user can configure the DS3/E3 Frame Generator/Frame Synchronizer blocks (within a particular channel) to operate in this orientation by writing the value "0xE6" into the "Mapper Control" register, as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

NOTES:

1. The number "N" (which is used in the address location for the "Mapper Control" Register ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).
2. In both of the above-mentioned Frame Generator/Frame Synchronizer Configurations, it is imperative that the user set the "TimRefSel[1:0]" bit-fields (within the "Operating Mode Register") to "[0, 1]" as depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	0	1

This particular setting configures the Frame Generator block to align its "Transmit Output DS3/E3 Frame Boundaries" with "Framing Alignment" information that will be provided to it from the Secondary Frame Synchronizer block. This will permit the "Frame Generator" block to generate frames that are "frame-aligned" with the incoming DS3/E3 Frames that the Secondary Frame Synchronizer block (which is typically upstream from the Frame Generator block) receives.

ONE FINAL NOTE: Between these two configurations Frame Generator/Frame Synchronizer Configuration # 28 is the most popular configuration, for normal applications. The reason for this is that Frame Generator/Frame Synchronizer Configuration # 28 permits the user to do full-blown Performance Monitoring on the Ingress Direction DS3/E3 Traffic (which has just been received from the remote DS3/E3 terminal equipment via coaxial cable).

Q8.5: What steps does one need to execute in order to (1) configure the DS3/E3 Framer block into a Framer Local Loop-back Mode, and (2) to enable the PRBS Pattern Generator and Receiver for diagnostic operation?

A8.5: This can be accomplished by either "looping the DS3/E3 data" on the "Line" (or Low-Speed Side of the XRT94L43) or on the "SONET/SDH" (or "High-Speed") Side. The procedure for performing this sort of diagnostic operation (in either direction) is presented below.

OPTION # 1 - To Loop the DS3/E3 Data on the Line (or Low-Speed) Side

STEP 1 – Configure a given channel to operate in the DS3/E3 Mode.
This is accomplished by setting bits 1 (Receive – Ingress – STS-1 Enable) and 0 (Transmit – Egress – STS-1 Enable), within the "Mapper Control" Register, each to "0", as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control Register – Byte 2" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 2 – Configure the Jitter Attenuator Blocks to be able to support DS3/E3 Signals
This can be accomplished by setting Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register – Byte 0" to "[0, X]" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	X	0	0	0	0	0

STEP 3 – Configure the DS3/E3 Framer Block to operate in Frame Generator/Frame Synchronizer Configuration # 28.
An illustration of "Frame Generator/Frame Synchronizer Configuration # 28, is presented below in Figure 8-3.

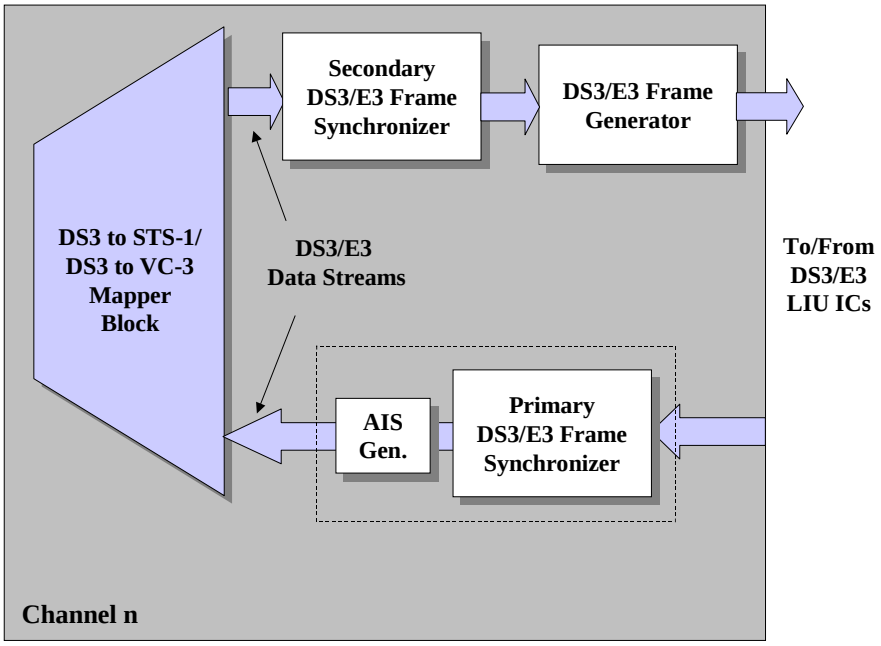

Figure 8-3, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 28"

NOTE: The user can execute STEP 3, by writing the value 0xE6 into the Mapper Control – T3/E3 Routing Register", as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control" Register – T3/E3 Routing Register" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 4 – Configure the DS3/E3 Framer Block to operate in the Local Loop-back Mode

Once the user accomplishes this, then all data that is output via the Frame Generator block, will (internally) be routed to the Receive Input of the Primary Frame Synchronizer block. Figure 8-4 presents an illustration of the DS3/E3 Framer block, operating in the Local Loop-back Mode.

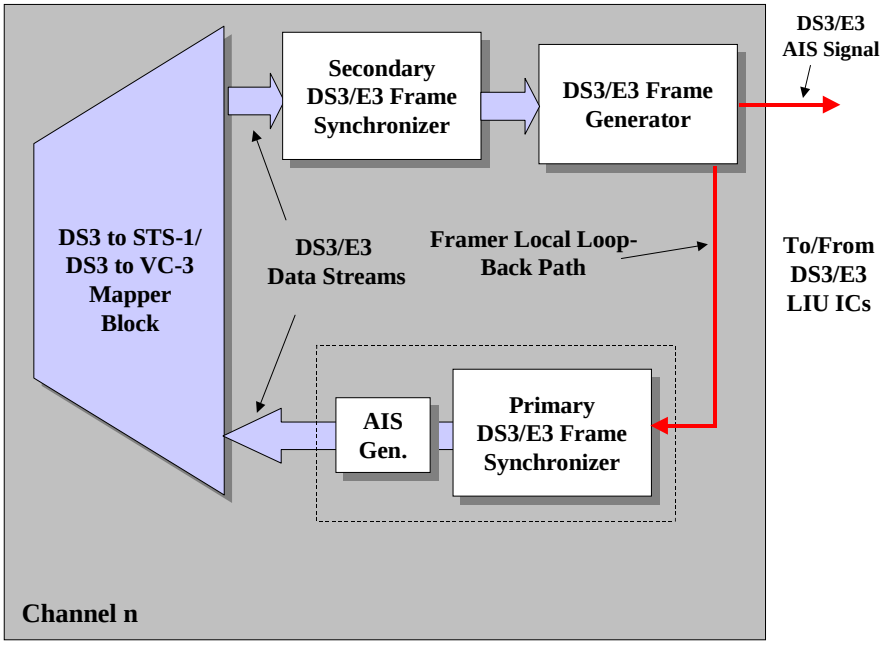

Figure 8-4, Illustration of the DS3/E3 Framer Block operating in the Local Loop-back Mode

NOTE: Whenever the DS3/E3 Framer block is configured to operate in the Local-Loop-back mode, the DS3/E3 Framer Generator block will automatically be configured to transmit a DS3/E3 AIS signal to the remote terminal (as indicated in Figure 8-4, above).

The user can configure the DS3/E3 Framer block to operate in the Local Loop-back Mode by setting Bit 7 (Local Loop-back) within the "Operating Mode" Register to "1" as depicted below.

Framer Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	1	1

NOTE: While writing data into this particular register, the user can also take this opportunity to configure the DS3/E3 Framer Block to operate in the "desired" Data-Rate/Framing Format. Table 8-1 presents the relationship between Bits 6 (IsDS3), Bit 2 (Frame Format) and the corresponding Data-Rate/Framing Format for the DS3/E3 Framer Block.

Table 8-1, The Relationship between Bits 6 (IsDS3), Bit 2 (Frame Format) and the Corresponding Data-Rate/Frame Format of the DS3/E3 Framer Block

Bit 6 (IsDS3)	Bit 2 (Frame Format)	Resulting Framing Format
0	0	E3, ITU-T G.751
0	1	E3, ITU-T G.832
1	0	DS3, C-bit Parity
1	1	DS3, M13

STEP 5 – Configure the Frame Generator block to operate in the "Local-Timing/Frame Slave" Mode.

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the

"up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 6 – Enable the PRBS Generator/Receiver within the DS3/E3 Framer Block
This is accomplished by setting bits 3 (RxPRBS Enable) and 2 (TxPRBS Enable) each to "1" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	1	1	0	0

NOTE: The PRBS Generator and Receiver are built right into the DS3/E3 Framer block. More specifically, the PRBS Generator block resides within the "Frame Generator" block, and the PRBS Receiver block resides within the "Primary Frame Synchronizer" block.

STEP 7 – Monitor the Performance of the DS3/E3 Framer Block.
At this point, the DS3/E3 Framer block should be configured into the Local Loop-back Mode. Further, the PRBS Generator and Receiver blocks should now be enabled and generating a "framed" PRBS pattern within DS3 or E3 traffic.

The next step is to monitor the performance and check for data integrity between the PRBS Pattern Generator and the PRBS Pattern Receiver.

This is achieved by doing the following.

STEP 7a – Check for DS3/E3 Framing Alignment
Depending upon the Data-Rate/Framing Format that the DS3/E3 Framer block is operating at, the user can check and determine whether or not the Primary Frame Synchronizer block is operating in the "In-Frame" state by checking the state of the appropriate register bit, as described below.

If the DS3/E3 Framer Block is operating in the DS3 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing the state of Bit 4 (RxOOF), within the "RxDS3 Configuration and Status" Register (as depicted below). If this bit-field is set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" condition.

Conversely, if this bit-field is set to "1", then the Primary Frame Synchronizer block is operating in the "Out of Frame" condition.

RxDS3 Configuration and Status Register (Indirect Address = 0xNE, 0x10; Direct Address = 0xNF10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxAIS	RxLOS	RxIdle	RxOOF	Unused	Framing with Valid P-Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	X	0	1	0	0

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.751 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.751 (as depicted below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 - G.751 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Unused		RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	0	0	1

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.751 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.832 (as depicted below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 – G.832 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPLD Unstab	RxTMark	RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	1	1	1

STEP 7b – Check for PRBS Lock

Once the user has confirmed that the Primary Frame Synchronizer block is operating in the "In-Frame" condition, then he/she can then check and determine whether or not the PRBS Receiver (within the Primary Frame Synchronizer block) is declaring "PRBS Lock" or not by testing the state of Bit 4 (RxPRBS Lock) within the "Test Register" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	X	1	1	0	0

If this bit-field is set to "1" then the PRBS Receiver is declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are receiving this "looped-back" Framed PRBS data in a somewhat error-free manner.

Conversely, if this bit-field is set to "0" then the PRBS Receiver is NOT declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are NOT receiving this "looped-back" Framed PRBS data in an error-free manner.

STEP 7c – Check for the occurrence of PRBS Errors

Finally, the user can determine the cumulative number of bit-errors that have been detected by the PRBS Receiver by reading out the contents of the PRBS Error Count Registers. The bit-format of the PRBS Error Count Register is presented below.

PRBS Error Count Register – MSB (Indirect Address = 0xNE, 0x68; Direct Address = 0xNF68)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PRBS Error Count Register – LSB (Indirect Address = 0xNE, 0x69; Direct Address = 0xNF69)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTES:

1. Since the PRBS Error Count Register is a 16-bit DS3/E3 Framer Block Register, then the user must read out the contents of these registers by first, reading out the contents of one of these registers. This will permit the user to obtain the contents of 8-bits of the "PRBS Error Count" Register. In order to obtain the contents of the other byte, then the user must read out the contents of the "PMON Holding Register". The bit-format and address location of the PMON Holding Register is presented below.

PMON Holding Register (Indirect Address = 0xNE, 0x6C; Direct Address = 0xNF6C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_Hold_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

2. The PRBS Error Count Registers are "Reset-upon-Read" type registers. Therefore, the contents of these registers reflect the number of PRBS errors that have been detected by the PRBS Receiver, since the last read of this register.
3. The user must make sure that the appropriate line rate clock signal is being applied into the Ingress Path of the Channel Under-Test. More specifically, if somebody wishes to operate this Framer Local Loop-back path in the DS3 Mode, then the user must make sure that a 44.736MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel. Likewise, if the user wishes to operate this Framer Local Loop-back Path in the E3 Mode, then the user must make sure that a 34.368MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel.

OPTION # 2 - To Loop the DS3/E3 Data on the SONET/SDH (or High-Speed) Side

STEP 1 – Configure a given channel to operate in the DS3/E3 Mode.
This is accomplished by setting bits 1 (Receive – Ingress – STS-1 Enable) and 0 (Transmit – Egress – STS-1 Enable), within the "Mapper Control" Register, each to "0", as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control Register – Byte 2" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 2 – Configure the Jitter Attenuator Blocks to be able to support DS3/E3 Signals
This can be accomplished by setting Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register – Byte 0" to "[0, X]" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	X	0	0	0	0	0

STEP 3 – Configure the DS3/E3 Framer Block to operate in Frame Generator/Frame Synchronizer Configuration # 23.
An illustration of "Frame Generator/Frame Synchronizer Configuration # 23, is presented below in Figure 8-5.

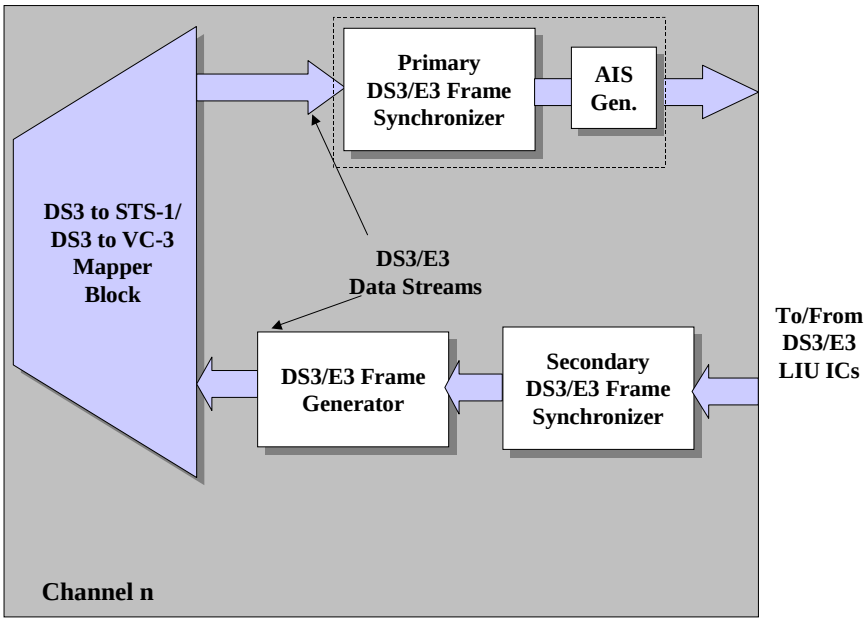

Figure 8-5, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 23"

NOTE: The user can execute STEP 3, by writing the value 0xC0 into the Mapper Control – T3/E3 Routing Register", as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control" Register – T3/E3 Routing Register" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 4 – Configure the DS3/E3 Framer Block to operate in the Local Loop-back Mode

Once the user accomplishes this, then all data that is output via the Frame Generator block, will (internally) be routed to the Receive Input of the Primary Frame Synchronizer block. Figure 8-6 presents an illustration of the DS3/E3 Framer block, operating in the Local Loop-back Mode.

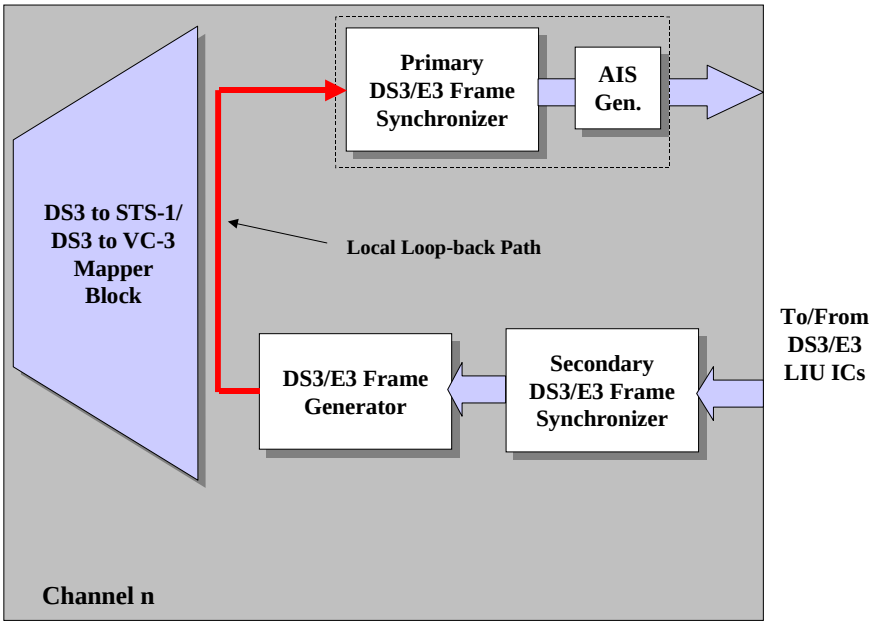

Figure 8-6, Illustration of the DS3/E3 Framer Block operating in the Local Loop-back Mode

The user can configure the DS3/E3 Framer block to operate in the Local Loop-back Mode by setting Bit 7 (Local Loop-back) within the "Operating Mode" Register to "1" as depicted below.

Framer Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	1	1

NOTE: While writing data into this particular register, the user can also take this opportunity to configure the DS3/E3 Framer Block to operate in the "desired" Data-Rate/Framing Format. Table 8-2 presents the relationship between Bits 6 (IsDS3), Bit 2 (Frame Format) and the corresponding Data-Rate/Framing Format for the DS3/E3 Framer Block.

Table 8-2, The Relationship between Bits 6 (IsDS3), Bit 2 (Frame Format) and the Corresponding Data-Rate/Frame Format of the DS3/E3 Framer Block

Bit 6 (IsDS3)	Bit 2 (Frame Format)	Resulting Framing Format
0	0	E3, ITU-T G.751
0	1	E3, ITU-T G.832
1	0	DS3, C-bit Parity
1	1	DS3, M13

STEP 5 – Configure the Frame Generator block to operate in the "Local-Timing/Frame Slave" Mode.

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the

"up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 6 – Enable the PRBS Generator/Receiver within the DS3/E3 Framer Block
This is accomplished by setting bits 3 (RxPRBS Enable) and 2 (TxPRBS Enable) each to "1" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	1	1	0	0

NOTE: The PRBS Generator and Receiver are built right into the DS3/E3 Framer block. More specifically, the PRBS Generator block resides within the "Frame Generator" block, and the PRBS Receiver block resides within the "Primary Frame Synchronizer" block.

STEP 7 – Monitor the Performance of the DS3/E3 Framer Block.
At this point, the DS3/E3 Framer block should be configured into the Local Loop-back Mode. Further, the PRBS Generator and Receiver blocks should now be enabled and generating a "framed" PRBS pattern within DS3 or E3 traffic.

The next step is to monitor the performance and check for data integrity between the PRBS Pattern Generator and the PRBS Pattern Receiver.

This is achieved by doing the following.

STEP 7a – Check for DS3/E3 Framing Alignment
Depending upon the Data-Rate/Framing Format that the DS3/E3 Framer block is operating at, the user can check and determine whether or not the Primary Frame Synchronizer block is operating in the "In-Frame" state by checking the state of the appropriate register bit, as described below.

If the DS3/E3 Framer Block is operating in the DS3 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing the state of Bit 4 (RxOOF), within the "RxDS3 Configuration and Status" Register (as depicted below). If this bit-field is set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" condition.

Conversely, if this bit-field is set to "1", then the Primary Frame Synchronizer block is operating in the "Out of Frame" condition.

RxDS3 Configuration and Status Register (Indirect Address = 0xNE, 0x10; Direct Address = 0xNF10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxAIS	RxLOS	RxIdle	RxOOF	Unused	Framing with Valid P-Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	X	0	1	0	0

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.751 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.751 (as depicted below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 - G.751 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Unused		RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	0	0	1

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.751 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.832 (as depicted below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 – G.832 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPLD Unstab	RxTMark	RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	1	1	1

STEP 7b – Check for PRBS Lock

Once the user has confirmed that the Primary Frame Synchronizer block is operating in the "In-Frame" condition, then he/she can then check and determine whether or not the PRBS Receiver (within the Primary Frame Synchronizer block) is declaring "PRBS Lock" or not by testing the state of Bit 4 (RxPRBS Lock) within the "Test Register" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	X	1	1	0	0

If this bit-field is set to "1" then the PRBS Receiver is declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are receiving this "looped-back" Framed PRBS data in a somewhat error-free manner.

Conversely, if this bit-field is set to "0" then the PRBS Receiver is NOT declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are NOT receiving this "looped-back" Framed PRBS data in an error-free manner.

STEP 7c – Check for the occurrence of PRBS Errors

Finally, the user can determine the cumulative number of bit-errors that have been detected by the PRBS Receiver by reading out the contents of the PRBS Error Count Registers. The bit-format of the PRBS Error Count Register is presented below.

PRBS Error Count Register – MSB (Indirect Address = 0xNE, 0x68; Direct Address = 0xNF68)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PRBS Error Count Register – LSB (Indirect Address = 0xNE, 0x69; Direct Address = 0xNF69)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTES:

1. Since the PRBS Error Count Register is a 16-bit DS3/E3 Framer Block Register, then the user must read out the contents of these registers by first, reading out the contents of one of these registers. This will permit the user to obtain the contents of 8-bits of the "PRBS Error Count" Register. In order to obtain the contents of the other byte, then the user must read out the contents of the "PMON Holding Register". The bit-format and address location of the PMON Holding Register is presented below.

PMON Holding Register (Indirect Address = 0xNE, 0x6C; Direct Address = 0xNF6C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_Hold_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

2. The PRBS Error Count Registers are "Reset-upon-Read" type registers. Therefore, the contents of these registers reflect the number of PRBS errors that have been detected by the PRBS Receiver, since the last read of this register.
3. The user must make sure that the appropriate line rate clock signal is being applied into the Ingress Path of the Channel Under-Test. More specifically, if somebody wishes to operate this Framer Local Loop-back path in the DS3 Mode, then the user must make sure that a 44.736MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel. Likewise, if the user wishes to operate this Framer Local Loop-back Path in the E3 Mode, then the user must make sure that a 34.368MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel.

Q8.6: What steps does one need to execute in order to (1) configure the XRT94L43 device into the Local Path Loop-back Mode, (2) to enable the PRBS Pattern Generator and Receiver (within the DS3/E3 Framer block), and (3) to check for proper data integrity between the PRBS Generator and PRBS Receiver?

A8.6: The user needs to execute the following steps.

STEP 1 – Configure a given channel to operate in the DS3/E3 Mode.
This is accomplished by setting bits 1 (Receive – Ingress – STS-1 Enable) and 0 (Transmit – Egress – STS-1 Enable), within the "Mapper Control" Register, each to "0", as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control Register – Byte 2" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 2 – Configure the Jitter Attenuator Blocks to be able to support DS3/E3 Signals.
This can be accomplished by setting Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register – Byte 0" to "[0, X]" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	X	0	0	0	0	0

STEP 3 – Configure the DS3/E3 Framer Block to operate in Frame Generator/Frame Synchronizer Configuration # 23.
An illustration of "Frame Generator/Frame Synchronizer" Configuration # 23 is presented below in Figure 8-7.

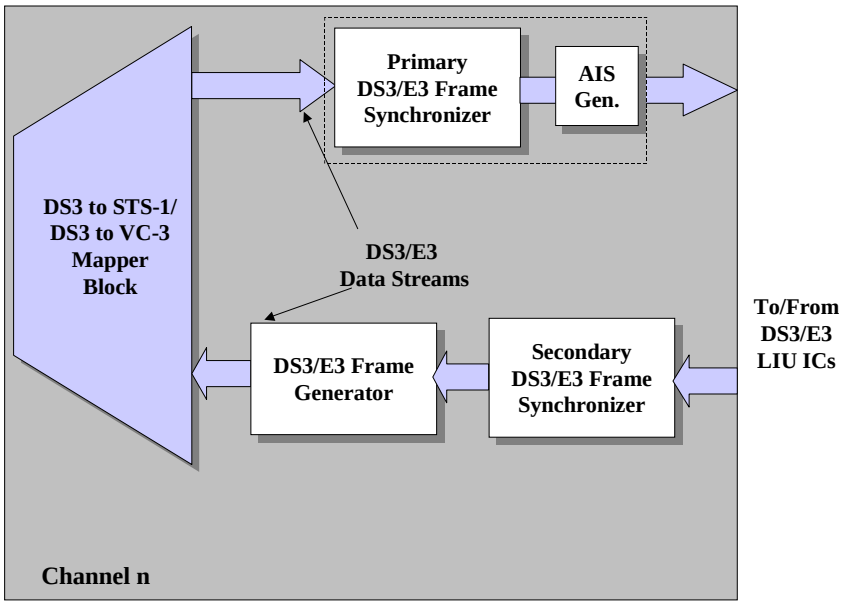

Figure 8-7, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 23"

NOTE: The user can execute STEP 3, by writing the value "0xC0" into the "Mapper Control – T3/E3 Routing Register" as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control" Register – T3/E3 Routing Register" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 4 – Configure the "DS3/E3 Framer" block to operate in the "desired" Data-Rate/Framing format.

This is accomplished by setting Bits 6 (IsDS3) and 2 (Frame Format) within the "Operating Mode Register" to the appropriate values, as presented below in Table 8-3. The bit-format of the "Operating Mode" Register, with these bit-fields "high-lighted" is also presented below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	X	1	0	1	X	1	1

Table 8-3, The Relationship between Bits 6 (IsDS3), Bit 2 (Frame Format) and the Corresponding Data-Rate/Frame Format of the DS3/E3 Framer Block

Bit 6 (IsDS3)	Bit 2 (Frame Format)	Resulting Framing Format
0	0	E3, ITU-T G.751
0	1	E3, ITU-T G.832
1	0	DS3, C-bit Parity
1	1	DS3, M13

STEP 5 – Configure the Frame Generator block to operate in the "Local Timing/Frame Slave" Mode.

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 6 - Invert the Clock (with respect to the DS3 Data) that is being generated by the Frame Generator Block.

This is accomplished by setting Bit 2 (DS3/E3 CLK OUT Invert) to "1" as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3 CLK OUT Invert	DS3/E3 CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	1	0	0

NOTE: This step is necessary if one intend to configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer Configuration # 23". This step will provide the Mapper Block will sufficient set-up and hold time with the DS3/E3 Data being generated by the Frame Generator block.

STEP 7 – Configure the XRT94L43 device to operate in the Local Path Loop-back Mode

Once the user accomplishes this, then all DS3/E3 data that is output via the Framer Generator block, will be routed through the "DS3/E3 Mapper" block (where this DS3/E3 signal will be mapped into an STS-1 SPE or a VC-3), and into the "Transmit SONET POH Processor" block. At this point, this STS-1 SPE or VC-3 data-stream will then be "looped-back" into the receive input of the "Receive SONET POH Processor" block. Afterwards, this STS-1 SPE or VC-3 data-stream will be routed to the "DS3/E3 Mapper" block (where the STS-1 SPEs/VC-3s will be terminated and the DS3/E3 data-stream will be extracted out). This DS3/E3 data-stream will then be routed into the Receive Input of the Primary Frame Synchronizer block. Figure 8-8 presents an illustration of a particular channel, operating in the Local Path Loop-back Mode.

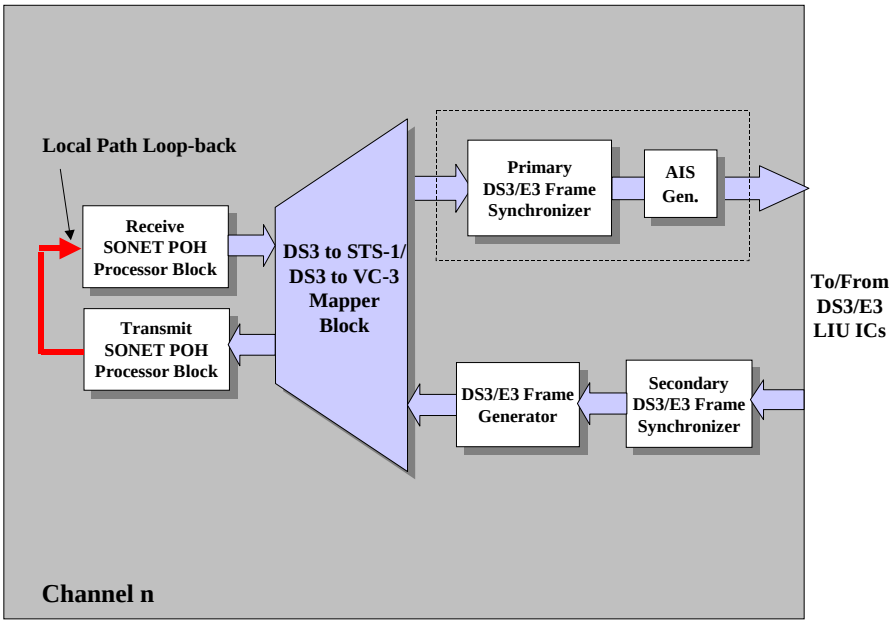

Figure 8-8, Illustration of the Channel operating in the Local Path Loop-back Mode

The user can configure the XRT94L43 device to operate in the Local Path Loop-back Mode by writing the value "0x03" into the "Loop-back Control Register – Byte 0" as depicted below.

Loop-back Control Register – Byte 0 (Indirect Address = 0x00, 0x1F; Direct Address = 0x011F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				Loop-back[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

NOTE: This register setting imposes "global" (not per-channel) configuration settings. Therefore, once the user executes this step, then all twelve (12) channels will be configured to operate in the "Local-Path Loop-back" Mode.

STEP 8 – Enable the PRBS Generator/Receiver within the DS3/E3 Framer Block
This is accomplished by setting bits 3 (RxPRBS Enable) and 2 (TxPRBS Enable) each to "1" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	1	1	0	0

NOTE: The PRBS Generator and Receiver are built right into the DS3/E3 Framer block. More specifically, the PRBS Generator block resides within the "Frame Generator" block, and the PRBS Receiver block resides within the "Primary Frame Synchronizer" block.

STEP 9 – Monitor the Data-Integrity/Performance of this Loop-back Path
At this point, the Channel should have been (1) configured to operate in the DS3/E3 Mode, and (2) configured to operate in the Local-Path Loop-back Mode. Further, the PRBS Generator and Receiver blocks should now be enabled and generating a "framed" PRBS pattern within DS3 or E3 traffic.

At this point, the user should begin to monitor the performance and check for data integrity between the PRBS Pattern Generator and the PRBS Pattern Receiver. Since this "Framed" PRBS data is traveling via the Local Path Loop-back Path, then the following entities are capable of doing Performance Monitoring.

- The Receive SONET POH Processor Block
- The Primary DS3/E3 Frame Synchronizer Block
- The PRBS Receiver Block (which resides within the Primary DS3/E3 Frame Synchronizer block).

The user can use these entities to do performance monitoring by doing the following.

STEP 9a – Confirm that the Receive SONET POH Processor block is properly receiving these STS-1 SPE/VC-3 frames.
This is accomplished by both checking for "Receive SONET POH Processor" block alarm conditions as well as the occurrence of B3 byte errors.

Checking for "Receive SONET POH Processor" block – type Alarms
The user can check for the occurrence of "Receive SONET POH Processor" block – type of alarms by periodically reading out the contents of both the "Receive SONET Path – Control Register – Byte 0" and the "Receive SONET Path – SONET Receive POH Status" Registers. The bit-format of each of these two registers is presented below.

Receive SONET Path – Control Register – Byte 0 (Indirect Address = 0xN0, 0x86; Direct Address = 0xN186)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						Async PDI-P State	J1 Unstable Indicator
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Receive SONET Path – SONET Receive POH Status – Byte 0 (Indirect Address = 0xN0, 0x87; Direct Address = 0xN187)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM-P Defect Declared	C2 Byte Unstable Condition	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

NOTES:
1. As long as the user reads out the value "0x00" for each of these registers, then the Receive SONET POH Processor block is NOT declaring any Alarm Conditions with the STS-1 SPE data that it is receiving from the Transmit SONET POH Processor block.

2. It is possible that (though not likely) that some of these alarm conditions could occur in a "somewhat" spurious manner, such that they would occur between READ operations to these registers (thereby causing the user to miss these alarm conditions). In this case, it might be better to rely upon the "Interrupt Status" Registers (which reflects the "latched" version of these alarm conditions) in order to determine if any of these alarm conditions have occurred since the last read of these registers. These Interrupt Status Registers, their address locations, and bit-formats are presented below.

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 2 (Indirect Address = 0xN0, 0x89; Direct Address = 0xN189)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change in PDI-P Condition Interrupt Status	Change in AIS-C Condition Interrupt Status	Change in LOP-C Condition Interrupt Status	Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	POH Capture Interrupt Status	Change in TIM-P Condition Interrupt Status	Change in J1 Unstable Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 1 (Indirect Address = 0xN0, 0x8A; Direct Address = 0xN18A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
New J1 Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Condition Interrupt Status	Change in PLM-P Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Condition Interrupt Status	Change in RDI-P Unstable Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 0 (Indirect Address = 0xN0, 0x8B; Direct Address = 0xN18B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Condition Interrupt Status	Change of AIS-P Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Checking for the occurrence of B3-byte errors

The user can check for the occurrence of B3 byte errors by either of the following two approaches.

- Checking for the occurrence of the "Detection of B3 Byte Error Interrupt", or
- Periodically reading out the contents of the "Receive SONET Path – B3 Error Count Registers.

The user can check for the occurrence of the "Detection of B3 Byte Error" Interrupt by periodically "polling" the state of Bit 7 (Detection of B3 Byte Error Interrupt Status), within the "Receive SONET Path – SONET Receive Path Interrupt Status – Byte 0" Register, as depicted below.

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 0 (Indirect Address = 0xN0, 0x8B; Direct Address = 0xN18B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Condition Interrupt Status	Change of AIS-P Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
X	0	0	0	0	0	0	0

If this bit-field is ever set to "1" then at least one B3 byte error has been detected (by the Receive SONET POH Processor block) since the last read of this register. Conversely, if this bit-field is set to "0" then the user can take some solace in knowing that no B3 byte errors have been detected since the last read of this register.

As mentioned earlier, the user can also check for the occurrence of B3 byte errors by reading out the contents of the "Receive SONET Path – B3 Error Count Register – Bytes 3 through 0". This is a 32-bit "Reset-upon-Read" register that contains the number of B3 errors that have been detected since the last read of these registers. The Address Location and Bit-Format for these registers is presented below.

Receive SONET Path – B3 Error Count Register – Byte 3 (Indirect Address = 0xN0, 0x98; Direct Address = 0xN198)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – B3 Error Count Register – Byte 2 (Indirect Address = 0xN0, 0x99; Direct Address = 0xN199)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – B3 Error Count Register – Byte 1 (Indirect Address = 0xN0, 0x9A; Direct Address = 0xN19A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – B3 Error Count Register – Byte 0 (Indirect Address = 0xN0, 0x9B; Direct Address = 0xN19B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTE: In order to properly read out these registers, the user should read out these Registers, in the following order.

- Receive SONET Path – B3 Error Count Register – Byte 3 (This register contains the Most Significant Byte for this 32-bit expression)
- Receive SONET Path – B3 Error Count Register – Byte 2
- Receive SONET Path – B3 Error Count Register – Byte 1
- Receive SONET Path – B3 Error Count Register – Byte 0 (This register contains the Least Significant Byte for this 32-bit expression)

STEP 9b – Check for DS3/E3 Framing Alignment

Depending upon the Data-Rate/Framing Format that the DS3/E3 Framer block is operating at, the user can check and determine whether or not the Primary Frame

Synchronizer block is operating in the "In-Frame" state by checking the state of the appropriate register bit, as described below.

If the DS3/E3 Framer Block is operating in the DS3 Framing Format

In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing the state of Bit 4 (RxOOF), within the "RxDS3 Configuration and Status" Register (as depicted below). If this bit-field is set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" condition. Conversely, if this bit-field is set to "1", then the Primary Frame Synchronizer block is operating in the "Out of Frame" condition.

RxDS3 Configuration and Status Register (Indirect Address = 0xNE, 0x10; Direct Address = 0xNF10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxAIS	RxLOS	RxIdle	RxOOF	Unused	Framing with Valid P-Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	X	0	1	0	0

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.751 Framing Format

In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.751 (as depicted below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 - G.751 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Unused		RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	0	0	1

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.832 Framing Format

In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.832 (as depicted

below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 – G.832 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPLD Unstab	RxTMark	RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	1	1	1

STEP 9c – Check for PRBS Lock

Once the user has confirmed that the Primary Frame Synchronizer block is operating in the "In-Frame" condition, then he/she can then check and determine whether or not the PRBS Receiver (within the Primary Frame Synchronizer block) is declaring "PRBS Lock" or not by testing the state of Bit 4 (RxPRBS Lock) within the "Test Register" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	X	1	1	0	0

If this bit-field is set to "1" then the PRBS Receiver is declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are receiving this "looped-back" Framed PRBS data in a somewhat error-free manner.

Conversely, if this bit-field is set to "0" then the PRBS Receiver is NOT declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are NOT receiving this "looped-back" Framed PRBS data in an error-free manner.

STEP 9d – Check for the occurrence of PRBS Errors

Finally, the user can determine the cumulative number of bit-errors that have been detected by the PRBS Receiver by reading out the contents of the PRBS Error Count Registers. The bit-format of the PRBS Error Count Register is presented below.

PRBS Error Count Register – MSB (Indirect Address = 0xNE, 0x68; Direct Address = 0xNF68)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PRBS Error Count Register – LSB (Indirect Address = 0xNE, 0x69; Direct Address = 0xNF69)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTES:

1. Since the PRBS Error Count Register is a 16-bit DS3/E3 Framer Block Register, then the user must read out the contents of these registers by first, reading out the contents of one of these registers. This will permit the user to obtain the contents of 8-bits of the "PRBS Error Count" Register. In order to obtain the contents of the other byte, then the user must read out the contents of the "PMON Holding Register". The bit-format and address location of the PMON Holding Register is presented below.

PMON Holding Register (Indirect Address = 0xNE, 0x6C; Direct Address = 0xNF6C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_Hold_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

2. The PRBS Error Count Registers are "Reset-upon-Read" type registers. Therefore, the contents of these registers reflect the number of PRBS errors that have been detected by the PRBS Receiver, since the last read of this register.
3. The user must make sure that the appropriate line rate clock signal is being applied to the Ingress Path of the Channel Under-Test. More specifically, if somebody wishes to operate this Local Path Loop-back path in the DS3 Mode, then the user must make sure that a 44.736MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel. Likewise, if the user wishes to operate this Local Path Loop-back Path in the E3 Mode, then the user must make sure that a 34.368MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel.

Q8.7: What steps does one need to execute in order to (1) configure the XRT94L43 device into the Local Transport Loop-back Mode, (2) to enable the PRBS Pattern Generator and Receive (within the DS3/E3 Framer block), and (3) to check for proper data integrity between the PRBS Generator and PRBS Receiver?

A8.7: The user needs to execute the following steps.

STEP 1 – Configure a given channel to operate in the DS3/E3 Mode
This is accomplished by setting bits 1 (Receive – Ingress – STS-1 Enable) and 0 (Transmit – Egress – STS-1 Enable), within the "Mapper Control" Register, each to "0" as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control Register – Byte 2" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 2 – Configure the Jitter Attenuator Blocks to be able to support DS3/E3 Signals.
This can be accomplished by setting Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register – Byte 0" to "[0, X]" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	X	0	0	0	0	0

STEP 3 – Configure the DS3/E3 Framer Block to operate in Frame Generator/Frame Synchronizer Configuration # 23.
An illustration of "Frame Generator/Frame Synchronizer" Configuration # 23 is presented below in Figure 8-9.

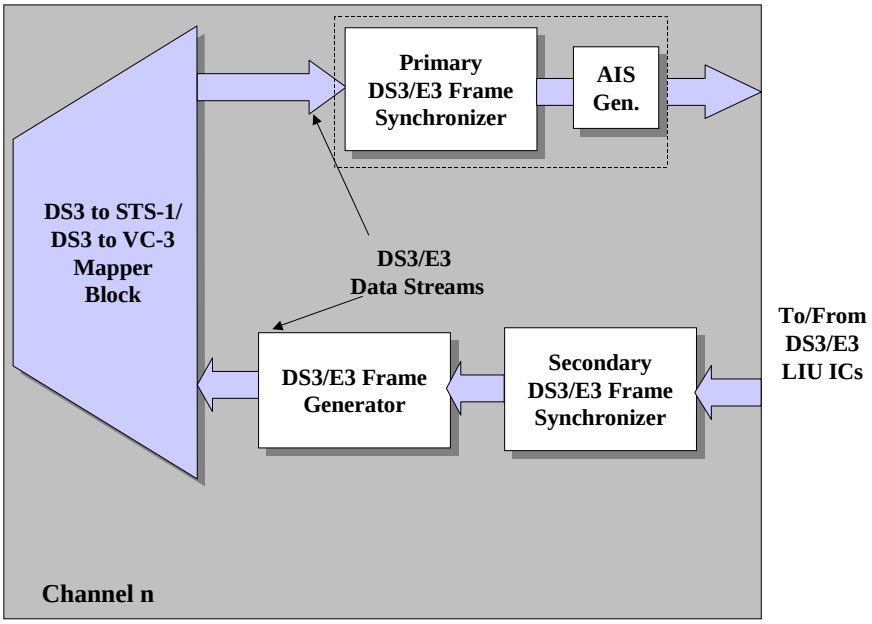

Figure 8-9, An Illustration of the "Frame Generator/Frame Synchronizer Configuration # 23"

NOTE: The user can execute STEP 3, by writing the value "0xC0" into the "Mapper Control – T3/E3 Routing Register" as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control" Register – T3/E3 Routing Register" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 4 – Configure the "DS3/E3 Framer" block to operate in the "desired" Data Rate/Framing format.

This is accomplished by setting Bits 6 (IsDS3) and 2 (Frame Format) within the "Operating Mode Register" to the appropriate values, as presented below in Table 8-3. The bit-format of the "Operating Mode" Register, with these bit-fields "high-lighted" is also presented below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	X	1	0	1	X	1	1

Table 8-4, The Relationship between Bits 6 (IsDS3), Bit 2 (Frame Format) and the Corresponding Data-Rate/Frame Format of the DS3/E3 Framer Block

Bit 6 (IsDS3)	Bit 2 (Frame Format)	Resulting Framing Format
0	0	E3, ITU-T G.751
0	1	E3, ITU-T G.832
1	0	DS3, C-bit Parity
1	1	DS3, M13

STEP 5 – Configure the Frame Generator block to operate in the "Local Timing/Frame Slave" Mode.

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 6 – Invert the Clock (with respect to the DS3 Data) that is being generated by the Frame Generator Block.

This is accomplished by setting Bit 2 (DS3/E3 CLK OUT Invert) to "1" as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3 CLK OUT Invert	DS3/E3 CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	1	0	0

NOTE: This step is necessary if one intend to configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer Configuration # 23". This step will provide the Mapper Block will sufficient set-up and hold time with the DS3/E3 Data being generated by the Frame Generator block.

STEP 7- Configure the XRT94L43 device to operate in the Local Transport Loop-back Mode

Once the user accomplishes this, then all DS3/E3 data that is output via the Frame Generator block, will be routed through the "DS3/E3 Mapper" block (where this DS3/E3 signal) will be mapped into an STS-1 SPE or a VC-3), and into the "Transmit SONET POH Processor" block. Afterwards, this particular STS-1 SPE (which contains our DS3/E3 data-stream) will be routed to the Transmit STS-12 TOH Processor block; where it will be "byte-interleaved" with eleven (11) other STS-1 SPE signal, and combined into an STS-12 signal. At this point, this STS-12 signal will then be "looped-back" into the

receive input of the "Receive STS-12 TOH Processor" block. Once this signal arrives at the "Receive STS-12 TOH Processor block, this STS-12 signal will be byte-de-interleaved into twelve STS-1 SPEs or AU-3/VC-3s. Each of these STS-1 SPEs or AU-3/VC-3s will be routed to their own corresponding Receive SONET POH Processor blocks. Afterwards, each of these STS-1 SPE or VC-3 data-stream (including the one carrying the DS3/E3 data-stream) will be routed to their corresponding "DS3/E3 Mapper" blocks (where the STS-1 SPE/VC-3s will be terminated and the DS3/E3 data-stream will be extracted out). Within the "Channel of Interest", this DS3/E3 data-stream will then be routed to the Receive Input of the Primary Frame Synchronizer block. Figure 8-10 presents an illustration of a particular channel, operating in the Local Transport Loop-back Mode.

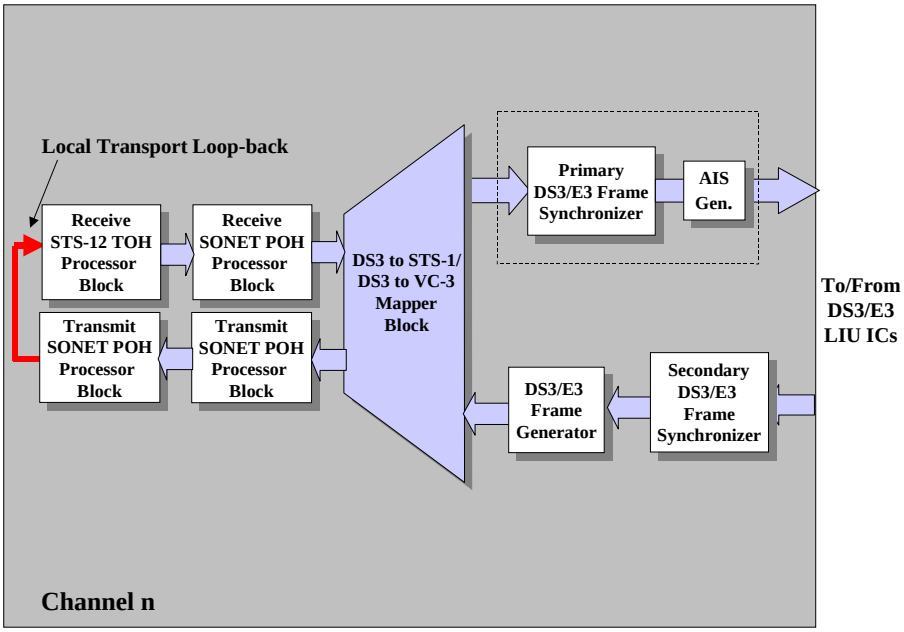

Figure 8-10, Illustration of the Channel operating in the Local Transport Loop-back Mode

The user can configure the XRT94L43 device to operate in the Local Transport Loop-back Mode by writing the value "0x02" into the "Loop-back Control Register – Byte 0" as depicted below.

Loop-back Control Register – Byte 0 (Indirect Address = 0x00, 0x1F; Direct Address = 0x011F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				Loop-back[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	0

STEP 8 – Enable the PRBS Generator/Receiver within the DS3/E3 Framer Block
This is accomplished by setting Bits 3 (RxPRBS Enable) and 2 (TxPRBS Enable) each to "1" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	1	1	0	0

NOTE: The PRBS Generator and Receiver are built right into the DS3/E3 Framer block. More specifically, the PRBS Generator block resides within the "Frame Generator" block, and the PRBS Receiver block resides within the "Primary Frame Synchronizer" block.

STEP 9 – Monitor the Data-Integrity/Performance of this Loop-back Path
At this point, the Channel should have been (1) configured to operate in the DS3/E3 Mode, and (2) configured to operate in the Local Transport loop-back Mode. Further, the PRBS Generator and Receiver blocks should now be enabled and generating a "framed" PRBS pattern within DS3 or E3 traffic.

At this point, the Channel should have been (1) configured to operate in the DS3/E3 Mode, and (2) configured to operate in the Local Transport Loop-back Mode. Further, the PRBS Generator and Receiver blocks should now be enabled and generating a "framed" PRBS pattern within DS3 or E3 traffic.

At this point, the user should begin to monitor the performance and check for data integrity between the PRBS Pattern Generator and the PRBS Pattern Receiver. Since this "Framed" PRBS data is traveling via the Local Transport Loop-back path, then the following entities are capable of doing Performance Monitoring.

- The Receive STS-12 TOH Processor Block
- The Receive SONET POH Processor Block
- The Primary DS3/E3 Frame Synchronizer Block
- The PRBS Receiver Block (which resides within the Primary DS3/E3 Frame Synchronizer block).

The user can use these entities to do performance monitoring by doing the following.

STEP 9a – Confirm that the Receive STS-12 TOH Processor block is properly receiving these incoming STS-12/STM-4 frames.
This is accomplished by both checking for "Receive STS-12 TOH Processor" block alarm conditions as well as the occurrence of B1 and B2 byte errors.

Checking for "Receive STS-12 TOH Processor" block – type Alarms
The user can check for the occurrence of "Receive STS-12 TOH Processor" block – type of alarms by periodically reading out the contents of both the "Receive STS-12 Transport Status Register – Byte 1" and the "Receive STS-12 Transport Status Register – Byte 0". The bit-format of each of these two registers is presented below.

Receive STS-12 Transport Status Register – Byte 1 (Indirect Address = 0x04, 0x06; Direct Address = 0x0506)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused					J0 Message Mismatch	J0 Message Unstable	AIS_L Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Receive STS-12 Transport Status Register – Byte 0 (Indirect Address = 0x04, 0x07; Direct Address = 0x0507)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDI-L Declared	S1 Unstable	K1, K2 (APS) Byte Unstable	SF Declared	SD Declared	LOF Defect Declared	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

NOTES:

1. As long the user reads out the value "0x00" for each of these registers, then the Receive STS-12 TOH Processor block is NOT declaring any Alarm Conditions with the STS-12 data that it is receiving from the Transmit STS-12 TOH Processor block.
2. It is possible that (though not likely) that some of these alarm conditions could occur in a "somewhat" spurious manner, such that they would occur between READ operations to these registers (thereby causing the user to miss these alarm conditions). In this case, it might be better to rely upon the "Interrupt Status" Registers (which reflects the "latched" version of these alarm conditions) in order to determine if any of these alarm conditions have occurred since the last read of these registers. These Interrupt Status Registers, their address locations, and bit-formats are presented below.

Receive STS-12 Transport Interrupt Status Register – Byte 2 (Indirect Address = 0x04, 0x09; Direct Address = 0x0509)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						Change of AIS-L Condition Interrupt Status	Change of RDI-L Condition Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport Interrupt Status Register – Byte 1 (Indirect Address = 0x04, 0x0A; Direct Address = 0x050A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
New S1 Byte Interrupt Status	Change in S1 Unstable State Interrupt Status	Change in J0 Message Unstable State Interrupt Status	New J0 Message Interrupt Status	Change in J0 Mismatch Condition Interrupt Status	Receive TOH CAP DONE Interrupt Status	Change in K1, K2 (APS) Bytes Unstable State Interrupt Status	NEW K1K2 Byte Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport Interrupt Status Register – Byte 0 (Indirect Address = 0x04, 0x0B; Direct Address = 0x050B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change in SF Condition Interrupt Status	Change in SD Condition Interrupt Status	Detection of REI-L Error Interrupt Status	Detection of B2 Error Interrupt Status	Detection of B1 Error Interrupt Status	Change of LOF Condition Interrupt Status	Change of SEF Condition Interrupt Status	Change of LOS Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Checking for the occurrence of B1 and B2 byte errors

The user can check for the occurrence of B1 and B2 byte errors by either of the following approaches.

- Checking for the occurrence of the "Detection of B1 Byte Error" and "Detection of B2 Byte Error" Interrupts, or
- Periodically reading out the contents of the "Receive STS-12 Transport – B1 Error Count" and "Receive STS-12 Transport – B2 Error Count" Registers.

The user can check for the occurrence of the "Detection of B1 Byte Error" and "Detection of B2 Byte Error" Interrupts by periodically

Receive STS-12 Transport Interrupt Status Register – Byte 0 (Indirect Address = 0x04, 0x0B; Direct Address = 0x050B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change in SF Condition Interrupt Status	Change in SD Condition Interrupt Status	Detection of REI-L Error Interrupt Status	Detection of B2 Error Interrupt Status	Detection of B1 Error Interrupt Status	Change of LOF Condition Interrupt Status	Change of SEF Condition Interrupt Status	Change of LOS Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	X	X	0	0	0

If either of these bit-fields are ever set to "1" then at least one B1 or B2 byte error has been detected (by the Receive STS-12 TOH Processor block) since the last read of this register. Conversely, if both of these bit-fields are set to "0" then the user can take some solace in knowing that no B1 or B2 byte errors have been detected since the last read of this register.

As mentioned earlier, the user can also check for the occurrence of B1 and B2 byte errors by reading out the contents of the "Receive STS-12 Transport – B1 Error Count" and

"Receive STS-12 Transport – B2 Error Count" Registers – Bytes 3 through 0. Each of these are a 32-bit Reset-upon-Read" register that contains the number of B1 or B2 errors that have been detected since the last read of these registers. The Address Location and Bit-Format for these registers is presented below.

Receive STS-12 Transport – B1 Error Count Register – Byte 3 (Indirect Address = 0x04, 0x10; Direct Address = 0x0510)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport – B1 Error Count Register – Byte 2 (Indirect Address = 0x04, 0x11; Direct Address = 0x0511)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport – B1 Error Count Register – Byte 1 (Indirect Address = 0x04, 0x12; Direct Address = 0x0512)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport – B1 Error Count Register – Byte 0 (Indirect Address = 0x04, 0x13; Direct Address = 0x0513)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTE: In order to properly read out these registers, the user should read out these Registers, in the following order.

- Receive STS-12 Transport – B1 Error Count Register – Byte 3 (This register contains the Most Significant Byte for this 32-bit expression)
- Receive STS-12 Transport – B1 Error Count Register – Byte 2
- Receive STS-12 Transport – B1 Error Count Register – Byte 1
- Receive STS-12 Transport – B1 Error Count Register – Byte 0 (This register contains the Least Significant Byte for this 32-bit expression).

Receive STS-12 Transport – B2 Error Count Register – Byte 3 (Indirect Address = 0x04, 0x14; Direct Address = 0x0514)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B2_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport – B2 Error Count Register – Byte 2 (Indirect Address = 0x04, 0x15; Direct Address = 0x0515)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B2_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport – B2 Error Count Register – Byte 1 (Indirect Address = 0x04, 0x16; Direct Address = 0x0516)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B2_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive STS-12 Transport – B2 Error Count Register – Byte 0 (Indirect Address = 0x04, 0x17; Direct Address = 0x0517)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B2_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTE: In order to properly read out these registers, the user should read out these Registers, in the following order.

- Receive STS-12 Transport – B2 Error Count Register – Byte 3 (This register contains the Most Significant Byte for this 32-bit expression)
- Receive STS-12 Transport – B2 Error Count Register – Byte 2
- Receive STS-12 Transport – B2 Error Count Register – Byte 1
- Receive STS-12 Transport – B2 Error Count Register – Byte 0 (This register contains the Least Significant Byte for this 32-bit expression).

STEP 9b – Confirm that the Receive SONET POH Processor block is properly receiving these STS-1 SPE/VC-3 frames.
This is accomplished by both checking for "Receive SONET POH Processor" block alarm conditions as well as the occurrence of B3 byte errors.

Checking for "Receive SONET POH Processor" block – type Alarms
The user can check for the occurrence of "Receive SONET POH Processor" block – type of alarms by periodically reading out the contents of both the "Receive SONET Path – Control Register – Byte 0" and the "Receive SONET Path – SONET Receive POH Status" Registers. The bit-format of each of these two registers is presented below.

Receive SONET Path – Control Register – Byte 0 (Indirect Address = 0xN0, 0x86; Direct Address = 0xN186)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						Async PDI-P State	J1 Unstable Indicator
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Receive SONET Path – SONET Receive POH Status – Byte 0 (Indirect Address = 0xN0, 0x87; Direct Address = 0xN187)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM-P Defect Declared	C2 Byte Unstable Condition	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

NOTES:
1. As long as the user reads out the value "0x00" for each of these registers, then the Receive SONET POH Processor block is NOT declaring any Alarm Conditions with the STS-1 SPE data that it is receiving from the Transmit SONET POH Processor block.
2. It is possible that (though not likely) that some of these alarm conditions could occur in a "somewhat" spurious manner, such that they would occur between READ operations to these registers (thereby causing the user to miss these alarm conditions). In this case, it might be better to rely upon the "Interrupt Status" Registers (which reflects the "latched" version of these alarm conditions) in order to determine if any of these alarm conditions have occurred since the last read of

these registers. These Interrupt Status Registers, their address locations, and bit-formats are presented below.

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 2 (Indirect Address = 0xN0, 0x89; Direct Address = 0xN189)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Change in PDI-P Condition Interrupt Status	Change in AIS-C Condition Interrupt Status	Change in LOP-C Condition Interrupt Status	Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	POH Capture Interrupt Status	Change in TIM-P Condition Interrupt Status	Change in J1 Unstable Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 1 (Indirect Address = 0xN0, 0x8A; Direct Address = 0xN18A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
New J1 Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Condition Interrupt Status	Change in PLM-P Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Condition Interrupt Status	Change in RDI-P Unstable Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 0 (Indirect Address = 0xN0, 0x8B; Direct Address = 0xN18B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Condition Interrupt Status	Change of AIS-P Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Checking for the occurrence of B3-byte errors

The user can check for the occurrence of B3 byte errors by either of the following two approaches.

- Checking for the occurrence of the “Detection of B3 Byte Error Interrupt”, or

• Periodically reading out the contents of the "Receive SONET Path – B3 Error Count Registers.

The user can check for the occurrence of the "Detection of B3 Byte Error" Interrupt by periodically "polling" the state of Bit 7 (Detection of B3 Byte Error Interrupt Status), within the "Receive SONET Path – SONET Receive Path Interrupt Status – Byte 0" Register, as depicted below.

Receive SONET Path – SONET Receive Path Interrupt Status – Byte 0 (Indirect Address = 0xN0, 0x8B; Direct Address = 0xN18B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Condition Interrupt Status	Change of AIS-P Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
X	0	0	0	0	0	0	0

If this bit-field is ever set to "1" then at least one B3 byte error has been detected (by the Receive SONET POH Processor block) since the last read of this register. Conversely, if this bit-field is set to "0" then the user can take some solace in knowing that no B3 byte errors have been detected since the last read of this register.

As mentioned earlier, the user can also check for the occurrence of B3 byte errors by reading out the contents of the "Receive SONET Path – B3 Error Count Register – Bytes 3 through 0". This is a 32-bit "Reset-upon-Read" register that contains the number of B3 errors that have been detected since the last read of these registers. The Address Location and Bit-Format for these registers is presented below.

Receive SONET Path – B3 Error Count Register – Byte 3 (Indirect Address = 0xN0, 0x98; Direct Address = 0xN198)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – B3 Error Count Register – Byte 2 (Indirect Address = 0xN0, 0x99; Direct Address = 0xN199)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – B3 Error Count Register – Byte 1 (Indirect Address = 0xN0, 0x9A; Direct Address = 0xN19A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Receive SONET Path – B3 Error Count Register – Byte 0 (Indirect Address = 0xN0, 0x9B; Direct Address = 0xN19B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTE: In order to properly read out these registers, the user should read out these Registers, in the following order.

- Receive SONET Path – B3 Error Count Register – Byte 3 (This register contains the Most Significant Byte for this 32-bit expression)
- Receive SONET Path – B3 Error Count Register – Byte 2
- Receive SONET Path – B3 Error Count Register – Byte 1
- Receive SONET Path – B3 Error Count Register – Byte 0 (This register contains the Least Significant Byte for this 32-bit expression)

STEP 9c – Check for DS3/E3 Framing Alignment

Depending upon the Data-Rate/Framing Format that the DS3/E3 Framer block is operating at, the user can check and determine whether or not the Primary Frame Synchronizer block is operating in the "In-Frame" state by checking the state of the appropriate register bit, as described below.

If the DS3/E3 Framer Block is operating in the DS3 Framing Format

In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing the state of Bit 4 (RxOOF), within the "RxDS3 Configuration and Status" Register (as depicted below). If this bit-field is set to

"0", then the Primary Frame Synchronizer block is operating in the "In-Frame" condition. Conversely, if this bit-field is set to "1", then the Primary Frame Synchronizer block is operating in the "Out of Frame" condition.

RxDS3 Configuration and Status Register (Indirect Address = 0xNE, 0x10; Direct Address = 0xNF10)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxAIS	RxLOS	RxIdle	RxOOF	Unused	Framing with Valid P-Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	X	0	1	0	0

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.751 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.751 (as depicted below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 - G.751 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Unused		RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	0	0	1

If the DS3/E3 Framer Block is operating in the E3, ITU-T G.832 Framing Format
In this case, the user can determine whether the Primary Frame Synchronizer block is operating in the "In-Frame" state by testing both the states of Bits 6 (RxLOF) and 5 (RxOOF), within the "RxE3 Configuration and Status" Register # 2 – G.832 (as depicted below). If both of these bit-fields are set to "0", then the Primary Frame Synchronizer block is operating in the "In-Frame" Condition. Conversely, if either one of these bits is set to "1", then the Primary Frame Synchronizer block is operating in either the "Loss of Frame" or "Out of Frame" condition.

RxE3 Configuration and Status Register # 2 – G.832 (Indirect Address = 0xNE, 0x11; Direct Address = 0xNF11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	RxPLD Unstab	RxTMark	RxFERF
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	X	X	0	0	1	1	1

STEP 9d – Check for PRBS Lock

Once the user has confirmed that the Primary Frame Synchronizer block is operating in the "In-Frame" condition, then he/she can then check and determine whether or not the PRBS Receiver (within the Primary Frame Synchronizer block) is declaring "PRBS Lock" or not by testing the state of Bit 4 (RxPRBS Lock) within the "Test Register" as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	X	1	1	0	0

If this bit-field is set to "1" then the PRBS Receiver is declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are receiving this "looped-back" Framed PRBS data in a somewhat error-free manner.

Conversely, if this bit-field is set to "0" then the PRBS Receiver is NOT declaring a "PRBS Lock" condition. This indicates that the PRBS Receiver (and Primary Frame Synchronizer block) are NOT receiving this "looped-back" Framed PRBS data in an error-free manner.

STEP 9e – Check for the occurrence of PRBS Errors

Finally, the user can determine the cumulative number of bit-errors that have been detected by the PRBS Receiver by reading out the contents of the PRBS Error Count Registers. The bit-format of the PRBS Error Count Register is presented below.

PRBS Error Count Register – MSB (Indirect Address = 0xNE, 0x68; Direct Address = 0xNF68)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PRBS Error Count Register – LSB (Indirect Address = 0xNE, 0x69; Direct Address = 0xNF69)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTES:

1. Since the PRBS Error Count Register is a 16-bit DS3/E3 Framer Block Register, then the user must read out the contents of these registers by first, reading out the contents of one of these registers. This will permit the user to obtain the contents of 8-bits of the "PRBS Error Count" Register. In order to obtain the contents of the other byte, then the user must read out the contents of the "PMON Holding Register". The bit-format and address location of the PMON Holding Register is presented below.

PMON Holding Register (Indirect Address = 0xNE, 0x6C; Direct Address = 0xNF6C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_Hold_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

2. The PRBS Error Count Registers are "Reset-upon-Read" type registers. Therefore, the contents of these registers reflect the number of PRBS errors that have been detected by the PRBS Receiver, since the last read of this register.
3. The user must make sure that the appropriate line-rate clock signal is being applied to the Ingress Path of the Channel Under-Test. More specifically, if somebody wishes to operate this Local Transport Loop-back path in the DS3 Mode, then the user must make sure that a 44.736MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel. Likewise, if the user wishes to operate this Local Transport Loop-back Path in the E3 Mode, then the user must make sure that a 34.368MHz clock signal is being provided to the Ingress Clock Input pin for this particular channel.

Q8.8: Can the DS3/E3 Framer blocks handle a Channelized DS3 data-stream that is of the M13/M23 Framing format?

A8.8: Yes, the DS3/E3 Framer block (within the XRT94L43 device) can be configured to handle a "Channelized DS3 data-stream" that is of the M13/M23 Framing Format. However, there are some steps that one must employ in order to make this work properly. All of these are described below.

THE ISSUE ASSOCIATED WITH CHANNELIZED DS3 DATA IN THE M13/M23 FRAMING FORMAT

If a given channelized DS3 data-stream is of the M13/M23 framing format, then there a couple facts to bear in mind.

1. The Frame Generator block (within the DS3/E3 Framer block) will (by default) set all of the C-bits (within an outbound DS3 signal, of the M13/M23 framing format) to "0".
2. The C-bits, within a Channelized DS3 data-stream that is of the M13/M23 framing format, reflect stuffing opportunities that either were, or were not taken (by the M23 Multiplexer) when multiplexing seven (7) DS2 signals into this DS3 signal. Therefore, these C-bits are very important in order to permit the M13 De-MUX to extract out the seven DS2 signals (and in turn the 28 DS1 signals) from this DS3 signal.

NOTE: None of this is an issue if this "Channelized" DS3 data-stream were in the C-Bit Parity Framing format.

As a consequence, if the user is not careful, a "Channelized DS3 signal (which is of the M13/M23 framing format) that is processed by the Frame Generator block will have all of its C-bits (within the overhead bits) set to "0". This situation could make the "DEMUX's" job (of extracting out the seven DS2 signals, in an un-erred manner) an impossible task.

Fortunately, the XRT94L43 device has a feature that permits the DS3/E3 Framer blocks to (1) process M13/M23 Channelized DS3 signals, and (2) still preserve the contents of the C-bits, as this data passes through the DS3/E3 Framer block. This feature is called the "Transmit Overhead Source" feature. If this feature is enabled, then the Frame Generator block will do the following.

1. It will accept the DS3 payload data via a "Payload Data Input Interface".
2. It will accept the DS3 overhead bits via the "Overhead Data Input Interface" and it will insert this overhead data into the "overhead bit" position, within the outbound DS3 data-stream.

THE TRANSMIT OVERHEAD SOURCE FEATURE IN USE:
Figure 8-11 presents an illustration of the DS3/E3 Framer block operating in "Frame Generator/Frame Synchronizer Configuration # 28". This figure indicates that any DS3/E3 data-stream, arriving at this channel, in the Egress Path will first pass through the "Secondary DS3/E3 Frame Synchronizer" block, and then the "DS3/E3 Frame Generator" block.

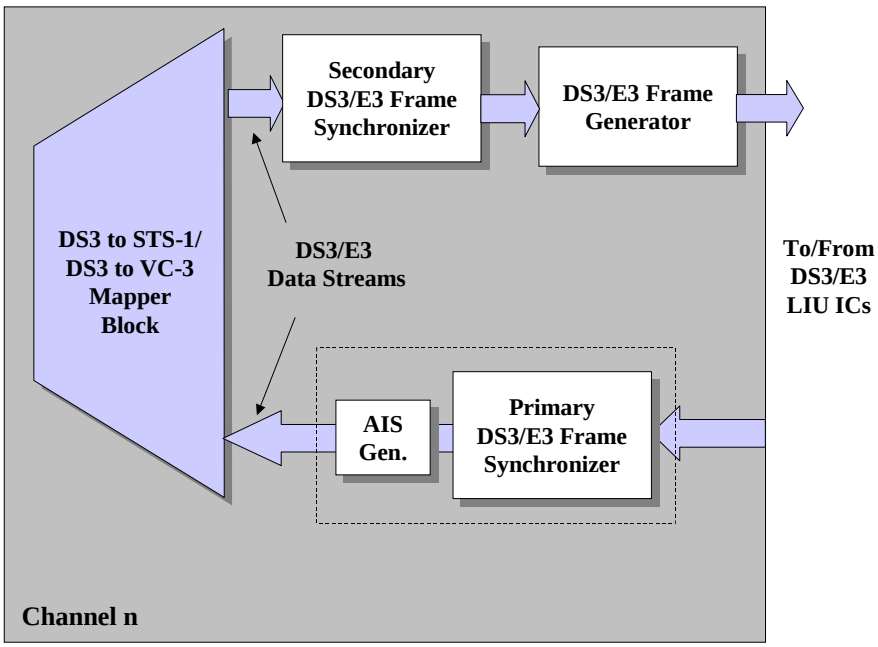

Figure 8-11, An Illustration of the DS3/E3 Framer Block operating in Frame Generator/Frame Synchronizer Configuration # 28

NOTE: The Primary Frame Synchronizer block does NOT alter the content of any DS3/E3 data that passes through it. Therefore, for the "0xE6 Configuration" there is no problem passing DS3 data through the DS3/E3 Framer block (in the Ingress Direction) in an "un-altered" manner. We only need to take steps to prevent the DS3/E3 Frame Generator block from altering the contents of the DS3 data in the Egress Direction. These remaining steps will address this concern.

The usefulness of the "Transmit Overhead Source" feature will become apparent, when analyzing the following two scenarios below.

When the "Transmit Overhead Source" Feature is disabled
Consider a "Channelized" DS3 data-stream (that is of the M13/M23 Framing format) that is de-mapped from SONET/SDH and is applied to the Egress Direction Input of the DS3/E3 Framer block, from the Mapper Block (as presented above in Figure 8-11). In this scenario, this DS3 data-stream will first arrive at and be processed by the "Secondary DS3/E3 Frame Synchronizer" block (which simply identifies the boundaries of each incoming DS3 frame, and flags defect conditions such as LOS, LOF or AIS). Afterwards, this DS3 data-stream will be routed to the "DS3/E3 Frame Generator" block for further processing. It should be noted that the Secondary DS3/E3 Frame Synchronizer block will NOT alter the contents of any DS3 data-bit (at all) as this DS3 data-stream is being processed through it.

After this DS3 data-stream leaves the "Secondary DS3/E3 Frame Synchronizer" block, it then arrives at the "DS3/E3 Frame Generator" block. This particular block is responsible for accepting the DS3 payload data from the "Secondary DS3/E3 Frame Synchronizer" block and computing and inserting the new DS3 overhead data into the outbound DS3 data-stream. If the DS3/E3 Framer block is configured to operate in the M13/M23 framing format, then it will be configured to (by default) set all of the C-bits (within the outbound DS3 data-stream – towards the LIU device) to "0".

As a consequence, all "DS2 Stuff indication" will have been removed from this DS3 data-stream, and the DE-MUX (which has the task of de-multiplexing this DS3 signal back into the seven DS2 signals) at the other end of the SONET network, will NOT be able to extract out these DS2 signals in an "error-free" manner.

When the "Transmit Overhead Source" Feature is enabled:
Consider a "Channelized" DS3 data-stream (that is of the M13/M23 Framing format) that is output form the Mapper block and is applied to the Egress Direction Input of the DS3/E3 Framer block (as presented in Figure 8-11). In this scenario, this "Egress-Direction" DS3 data-stream will first arrive at and be processed by the "Secondary

DS3/E3 Frame Synchronizer" block. Afterwards, this DS3 data-stream will be routed to the "DS3/E3 Frame Generator" block for further processing. It should be noted that the Secondary DS3/E3 Frame Synchronizer block will NOT alter the contents of any DS3 data-bit (at all) as this DS3 data-stream is being processed through it.

After this DS3 data-stream leaves the "Secondary DS3/E3 Frame Synchronizer" block, it then arrives at the "DS3/E3 Frame Generator" block. This particular block is responsible for accepting the DS3 payload data from the "Secondary DS3/E3 Frame Synchronizer" block and computing and inserting the new DS3 overhead data into the outbound DS3 data-stream. However, if the "Transmit Overhead Source" feature is enabled, then the "DS3/E3 Frame Generator" block will be configured to also accept the Overhead Bits from the "Secondary DS3/E3 Frame Synchronizer" block (upstream), and will insert these same overhead bit-values into the overhead bit-positions within the outbound DS3 data-stream. As a consequence, the contents of the overhead bits, within the DS3 data-stream that is output via the "DS3/E3 Frame Generator" block will be exactly the same as that which enters the "Secondary DS3/E3 Frame Synchronizer" block.

As a consequence, for a "Channelized/M13/M23" DS3 signal, the C-bit values will NOT be altered by the "DS3/E3 Frame Generator" block. Hence, the DS2 Stuff Indications (within this DS3 data-stream) are not removed from this DS3 data-stream. This will permit the DE-MUX (at the other end of the SONET network) to extract out the seven DS2 signals, in an un-erred manner.

ENABLING THE "TRANSMIT OVERHEAD SOURCE" FEATURE

The user can enable the "Transmit Overhead Source" feature by executing the following steps.

STEP 1 – Configure the Frame Generator block to operate in the "Local-Timing/Frame-Slave" Mode

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 2 – Set Bit 7 (TxOHSrc), within the "Test Register" to "1" as depicted below

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
1	0	0	0	0	0	0	0

Once the user executes this step, then the DS3/E3 Frame Generator block will be configured to accept the overhead bits from the Secondary DS3/E3 Frame Synchronizer block, and it will insert this data into the Overhead bit-positions within the outbound DS3 data-stream.

STEP 3 – Make sure that the Appropriate Set of the following (shaded) bits, within the next four registers (below) is set to "0" (the default value).

TxDS3 F-Bit Mask # 1 Register (Indirect Address = 0xNE, 0x36; Direct Address = 0xNF36)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				F_Bit Mask[27]/ UDL Bit # 9 (C73)	F_Bit Mask [26]/ UDL Bit # 8 (C72)	F_Bit Mask [25]/ UDL Bit # 7 (C71)	F_Bit Mask [24]/
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TxDS3 F-Bit Mask # 2 Register (Indirect Address = 0xNE, 0x37; Direct Address = 0xNF37)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_Bit Mask [23]/ UDL Bit # 6 (C63)	F_Bit Mask [22]/ UDL Bit # 5 (C62)	F_Bit Mask [21]/ UDL Bit # 4 (C61)	F_Bit Mask [20]	F_Bit Mask [19]/ DL Bit # 3 (C53)	F_Bit Mask [18]/ DL Bit # 2 (C52)	F_Bit Mask [17]/ DL Bit # 1 (C51)	F_Bit Mask [16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TxDS3 F-Bit Mask # 3 Register (Indirect Address = 0xNE, 0x38; Direct Address = 0xNF38)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_Bit Mask [15]/ FEBE Bit 3 (C43)	F_Bit Mask [14]/ FEBE Bit 2 (C42)	F_Bit Mask [13]/ FEBE Bit 1 (C41)	F_Bit Mask [12]	F_Bit Mask [11]/ CP Bit # 3 (C33)	F_Bit Mask [10]/ CP Bit # 2 (C32)	F_Bit Mask [9]/ CP Bit # 1 (C31)	F_Bit Mask [8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TxDS3 F-Bit Mask # 4 Register (Indirect Address = 0xNE, 0x39; Direct Address = 0xNF39)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_Bit Mask [7]/ UDL Bit # 3 (C23)	F_Bit Mask [6]/ UDL Bit # 2 (C22)	F_Bit Mask [5]/ UDL Bit # 1 (C21)	F_Bit Mask [4]/ X Bit # 2	F_Bit Mask [3]/ FEAC Bit (C13)	F_Bit Mask [2]/ NA Bit (C12)	F_Bit Mask [1]/ AIC Bit (C11)	F_Bit Mask [0]/ X Bit # 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This step configures the "DS3/E3 Frame Generator" block to accept the overhead data (from the Secondary DS3/E3 Frame Synchronizer" block) for these particular bit-fields, and to insert this data into the overhead bit-fields within the outbound DS3 data-stream.

NOTES:

1. If any of these bit-fields are set to "1", then the "DS3/E3 Frame Generator" block will NOT accept nor insert the overhead data (from the Secondary DS3/E3 Frame Synchronizer" block) into the overhead bit-positions that corresponds with that or those particular register bits.
2. If the user wishes to configure the "DS3/E3 Frame Generator" block to be able to automatically transmit the FERF (Far-End Receive Failure) condition, then the user should set Bits 4 (X Bit # 2) and 0 (X Bit # 1) within the "TxDS3 F-Bit Mask # 4 Register, to the value "1" as depicted below. This step will configure the "DS3/E3 Frame Generator" block to NOT accept nor insert data (from the Secondary DS3/E3 Frame Synchronizer" block) that corresponds to the "X-Bits".

TxDS3 F-Bit Mask # 4 Register (Indirect Address = 0xNE, 0x39; Direct Address = 0xNF39)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F_Bit Mask [7]/ UDL Bit # 3 (C23)	F_Bit Mask [6]/ UDL Bit # 2 (C22)	F_Bit Mask [5]/ UDL Bit # 1 (C21)	F_Bit Mask [4]/ X Bit # 2	F_Bit Mask [3]/ FEAC Bit (C13)	F_Bit Mask [2]/ NA Bit (C12)	F_Bit Mask [1]/ AIC Bit (C11)	F_Bit Mask [0]/ X Bit # 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	1

Q8.9: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 23" can the user configure the DS3/E3 Framer block to automatically transmit the DS3/E3 AIS indicator towards the Mapper block, in response to a defect being detected in the Ingress Direction?

A8.9: The answer to this question is "Yes". Let us presume that the LOS defect was detected within the Ingress DS3/E3 signal, by the Secondary DS3/E3 Frame Synchronizer block. If the user configured the XRT94L43 device accordingly, the DS3/E3 Frame Generator block will respond by automatically generating and transmitting the AIS condition (in the Ingress Direction) for the duration that this LOS defect exists.

Figure 8-12 presents an illustration of the DS3/E3 Framer block implementing this Defect Detection and AIS Transmission scheme.

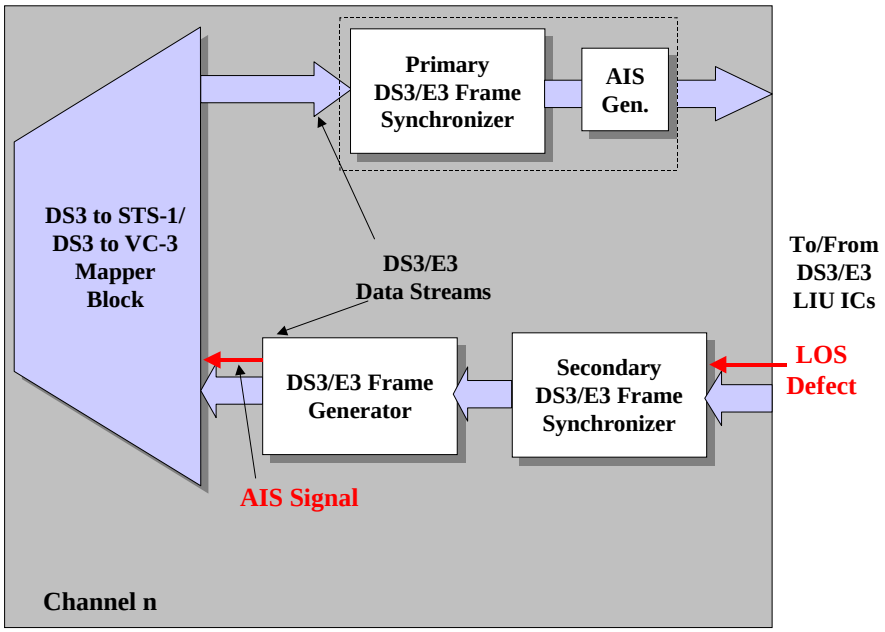

Figure 8-12, Illustration of the LOS Defect occurring within the Ingress Direction, and the resulting transmission of the AIS signal down-stream, towards the DS3/E3 Mapper block

NOTE: In this configuration, the Primary DS3/E3 Frame Synchronizer block will NOT respond by transmitting the FERF (DS3 RDI) indicator back out to the remote terminal equipment (e.g., the source of the defective DS3/E3 data) via the Egress Path.

Implementing this Defect/AIS Transmission Configuration

The user can configure this "defect-detection" and "automatic AIS transmission" feature by setting Bits 0 (Transmit AIS Down-stream upon AIS), 2 (Transmit AIS Down-stream upon LOF) and 4 (Transmit AIS Down-stream upon LOS), within the "Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block" to "1", as depicted below.

Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block (Indirect Address = 0xNE, 0xF2; Direct Address = 0xNFF2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	1	0	1

Q8.10: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 23" can the user configure the corresponding Transmit SONET POH Processor block to automatically transmit the PDI-P indicator, in response to a defect being detected in the Ingress Direction (by the DS3/E3 Framer block)?

A8.10: The answer to this question is "Yes". Let us presume that the LOS defect was detected within the Ingress DS3/E3 signal, by the Secondary DS3/E3 Frame Synchronizer block. If the user configured the XRT94L43 device accordingly, the corresponding Transmit SONET POH Processor block would respond by automatically generating and transmitting the PDI-P condition for the duration that this LOS defect exists.

NOTE: The Transmit SONET POH Processor block will transmit the PDI-P condition, by setting the C2 byte (of each outbound STS-1 SPE) to the value "0xFC".

Figure 8-13 presents an illustration of the XRT94L43 device implementing this Defect Detection and PDI-P Transmission Scheme.

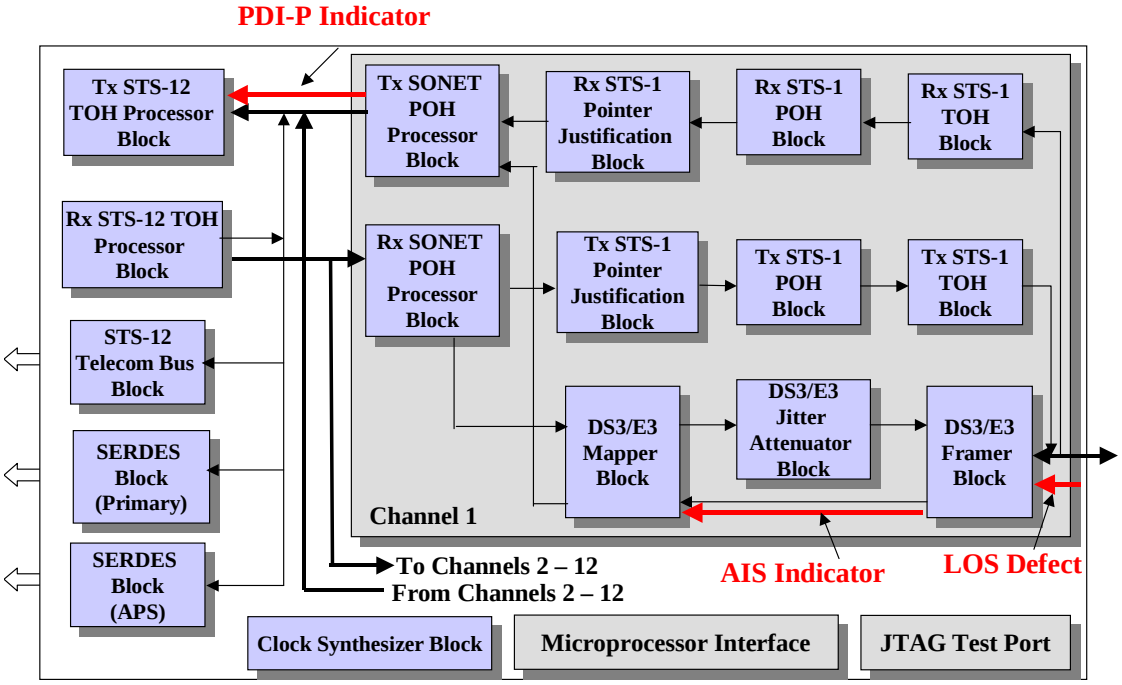

Figure 8-13, Illustration of the LOS Defect occurring within the Ingress Direction, and the resulting transmission of the PDI-P signal down-stream (towards the SONET Network).

Implementing this Defect/PDI-P Transmission Configuration

The user can configure this "defect-detection" and "automatic PDI-P transmission" feature by setting Bits 1 (Transmit PDI-P Down-stream upon AIS), 3 (Transmit PDI-P Down-stream upon LOF) and 5 (Transmit PDI-P Down-stream upon LOS), within the Receive DS3/E3 AIS/PDI-P Alarm Enable – Secondary Frame Synchronizer Block" Register; to "1" as depicted below.

Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block (Indirect Address = 0xNE, 0xF2; Direct Address = 0xNFF2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	0

NOTE: This particular register permits the user to configure the both the transmission of the AIS indicator (by the DS3/E3 Frame Generator block) as well as the transmission of the PDI-P (by the Transmit SONET POH Processor block) to occur simultaneously in response to any of the following defect conditions: LOS, LOF and AIS.

Q8.11: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 23" can the user configure the DS3/E3 block to automatically transmit the DS3/E3 AIS indicator (in the Egress Direction) in response to a defect being detected in the Egress DS3/E3 signal (coming from the DS3/E3 Mapper block)?

A8.11: The answer to this question is "Yes". Let us presume that the LOF defect was detected within the Egress DS3/E3 signal, by the Primary DS3/E3 Frame Synchronizer block. If the user configured the XRT94L43 device accordingly, the Primary DS3/E3 Frame Synchronizer block would respond by automatically turning on the "AIS Pattern Generator" for the duration that this LOF defect exists.

Figure 8-14 presents an illustration of the DS3/E3 Framer block implementing this Defect Detection and AIS Transmission scheme.

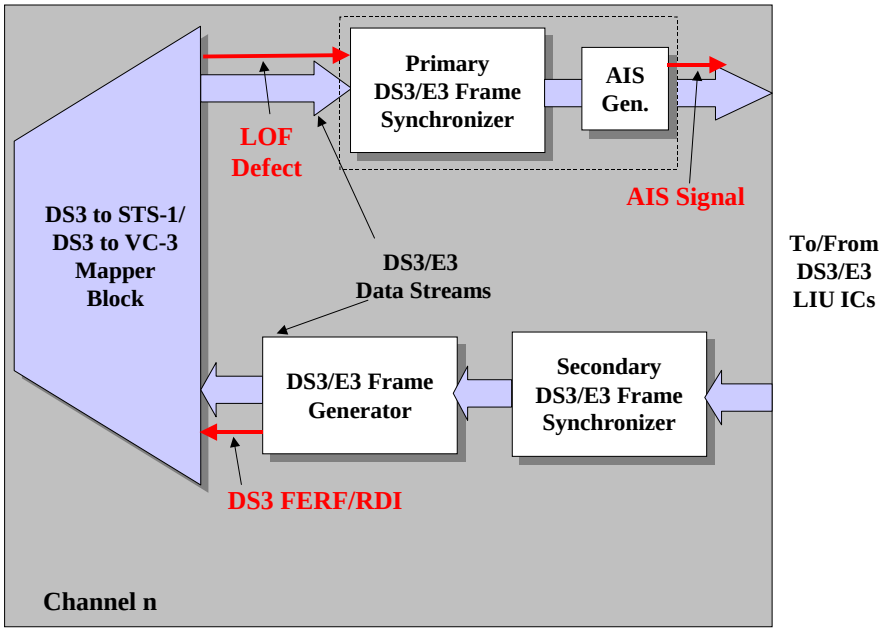

Figure 8-14, Illustration of the LOF Defect occurring within the Egress Direction, and the resulting transmission of the AIS signal down-stream, towards the DS3/E3 LIU Devices

NOTE: In this configuration, the DS3/E3 Frame Generator block will respond to this LOF defect by transmitting the FERF (DS3 RDI) indicator back out to source of this defective DS3 data via the Ingress Path (and through the SONET/SDH network).

Implementing this Defect/AIS Transmission Configuration

The user can configure this "defect-detection" and "automatic AIS transmission" feature by setting Bits 0 (Transmit AIS Down-stream upon AIS), 2 (Transmit AIS Down-stream upon LOF) and 4 (Transmit AIS Down-stream upon LOS), within the Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block; to "1", as depicted below.

Receive DS3/E3 AIS/PDI-P Alarm Enable Register - Secondary Frame Synchronizer Block (Indirect Address = 0xNE, 0xF2; Direct Address = 0xNFF2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	1	0	1

Q8.12: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 23" can the user configure the DS3/E3 block to automatically transmit the DS3/E3 AIS indicator (in the Egress Direction) in response to the corresponding Receive SONET POH Processor block declaring the PDI-P defect condition?

A8.12: The answer to this question is "Yes". Let us presume that the corresponding Receive SONET POH Processor block has detected the PDI-P indicator, within the STS-1 signal that it is receiving from the SONET/SDH Network. If the user configured the XRT94L43 device accordingly, the Primary Frame Synchronizer block would respond (to this detection of PDI-P) by automatically generating and transmitting the AIS signal (in the Egress Direction) for the duration that this PDI-P defect exists.

Figure 8-15 presents an illustration of the XRT94L43 device implementing this PDI-P Detection and resulting transmission of AIS scheme.

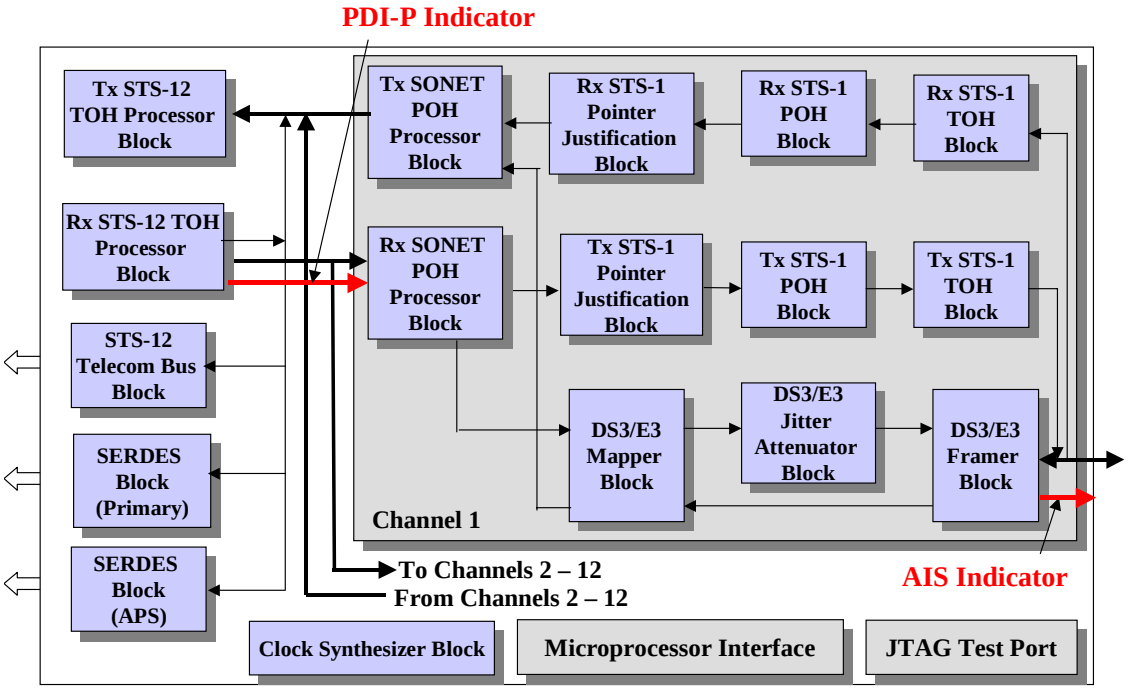

Figure 8-15, Illustration of the Receive SONET POH Processor block detecting the PDI-P condition, and the resulting transmission of the AIS signal down-stream (towards the DS3/E3 LIU devices)

Implementing this PDI-P Defect/AIS Transmission Configuration

The user can configure this "PDI-P Defect detection and "automatic AIS transmission feature by setting Bit 0 (Transmit DS3 AIS via Down-stream DS3) upon PDI-P), within the "Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0", as depicted below.

Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0 (Indirect Address = 0xN2, 0xC3; Direct Address = 0xN3C3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit AIS-P (via Downstream STS-1s) upon LOP-P	Unused	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	Unused	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	Transmit AIS-P (via Downstream STS-1s) upon AIS-P	Transmit DS3 AIS (via Downstream DS3) upon PDI-P
R/W	R/O	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

Q8.13: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 28" can the user configure the DS3/E3 Framer block to automatically transmit the DS3/E3 AIS Indicator towards the Mapper block, in response to a defect being detected in the Ingress Direction?

A8.13: The answer to this question is "Yes". Let us presume that the LOS defect was detected within the Ingress DS3/E3 signal, by the Primary DS3/E3 Frame Synchronizer block. If the user configured the XRT94L43 device accordingly, the Primary DS3/E3 Frame Synchronizer block will respond by automatically turning on the AIS Pattern Generator for the duration that this LOS defect exists.

Figure 8-16 presents an illustration of the DS3/E3 Framer block implementing this Defect Detection and AIS Transmission scheme.

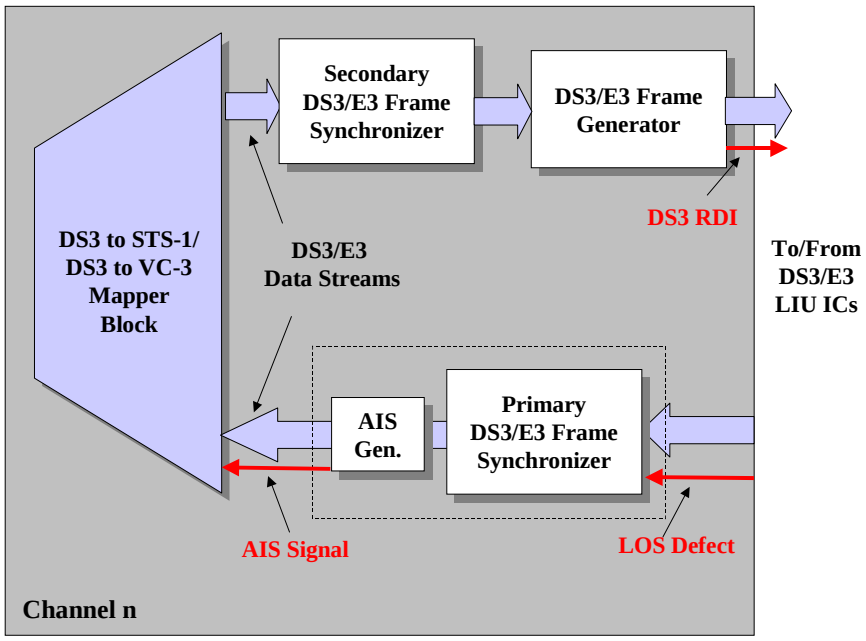

Figure 8-16, Illustration of the LOS Defect occurring within the Ingress Direction, and the resulting transmission of the AIS signal down-stream, towards the DS3/E3 Mapper block

NOTE: In this configuration, the DS3/E3 Frame Generator block will respond by transmitting the FERF (DS3 RDI) indicator back out to the remote terminal equipment via the Egress Path.

Implementing this Defect/AIS Transmission Configuration

The user can configure this "defect-detection" and "automatic AIS transmission" feature by setting Bits 0 (Transmit AIS Down-stream upon AIS), 2 (Transmit AIS Down-stream upon LOF) and 4 (Transmit AIS Down-stream upon LOS), within the "Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Primary Frame Synchronizer Block" to "1", as depicted below.

Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Primary Frame Synchronizer Block (Indirect Address = 0xNE, 0x4D; Direct Address = 0xNF4D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	1	0	1

Q8.14: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 28" can the user configure the corresponding Transmit SONET POH Processor block to automatically transmit the PDI-P indicator, in response to a defect being detected in the Ingress Direction (by the DS3/E3 Framer block)?

A8.14: The answer to this question is "Yes". Let us presume that the LOS defect was detected within the Ingress DS3/E3 signal, by the Primary DS3/E3 Frame Synchronizer block. If the user configured the XRT94L43 device accordingly, the Transmit SONET POH Processor block will respond by automatically generating and transmitting the PDI-P condition for the duration that this LOS defect exists.

NOTE: The Transmit SONET POH Processor block will transmit the PDI-P condition, by setting the C2 byte (of each outbound STS-1 SPE) to the value "0xFC".

Figure 8-17 presents an illustration of the XRT94L43 device implementing this Defect Detection and PDI-P Transmission Scheme.

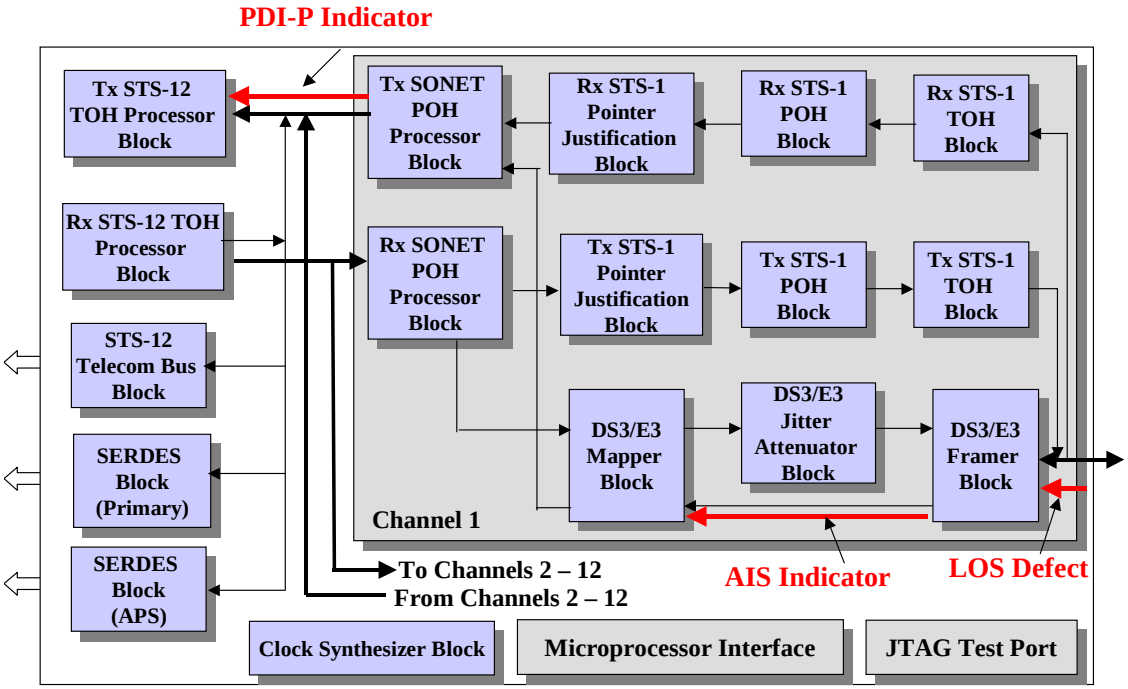

Figure 8-17, Illustration of the LOS Defect occurring within the Ingress Direction, and the resulting transmission of the PDI-P signal down-stream (towards the SONET Network).

Implementing this Defect/PDI-P Transmission Configuration

The user can configure this "defect-detection" and "automatic PDI-P transmission" feature by setting Bits 1 (Transmit PDI-P Down-stream upon AIS), 3 (Transmit PDI-P Down-stream upon LOF) and 5 (Transmit PDI-P Down-stream upon LOS), within the Receive DS3/E3 AIS/PDI-P Alarm Enable – Primary Frame Synchronizer Block" Register; to "1" as depicted below.

Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Primary Frame Synchronizer Block (Indirect Address = 0xNE, 0x4D; Direct Address = 0xNF4D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	0

NOTE: This particular register permits the user to configure the both the transmission of the AIS indicator (by the DS3/E3 Frame Generator block) as well as the transmission of the PDI-P (by the Transmit SONET POH Processor block) in response to any of the following defect conditions: LOS, LOF and AIS.

Q8.15: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 28" can the user configure the DS3/E3 block to automatically transmit the DS3/E3 AIS indicator (in the Egress Direction) in response to a defect being detected in the Egress DS3/E3 signal (coming from the DS3/E3 Mapper block)?

A8.15: The answer to this question is "Yes". Let us presume that the LOF defect was detected within the Egress (e.g., de-mapped) DS3/E3 signal, by the Secondary DS3/E3 Frame Synchronizer block. If the user configured the XRT94L43 device accordingly, the DS3/E3 Frame Generator block will respond by automatically generating and transmitting the AIS condition (in the Egress Direction) for the duration that this LOF defect exists.

Figure 8-18 presents an illustration of the DS3/E3 Framer block implementing this Defect Detection and AIS Transmission scheme.

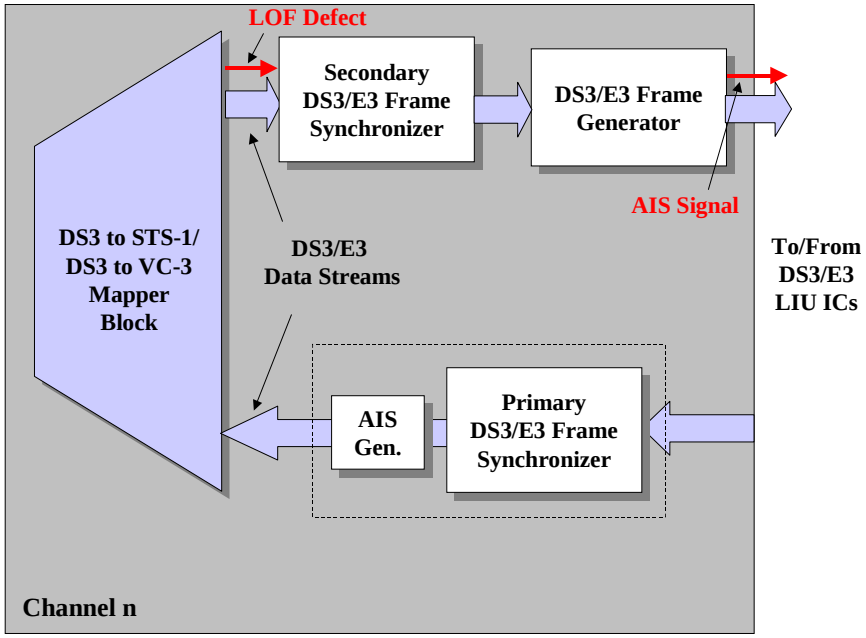

Figure 8-18, Illustration of the LOF Defect occurring within the Egress Direction, and the resulting transmission of the AIS signal down-stream towards ,the DS3/E3 LIU Devices

NOTE: In this configuration, the Primary DS3/E3 Frame Synchronizer block will NOT respond by transmitting the FERF (DS3 RDI) indicator back out to the source of the defective equipment (via the Ingress Path and the SONET/SDH Network).

Implementing this Defect/AIS Transmission Configuration

The user can configure this "defect-detection" and "automatic AIS transmission" feature by setting Bits 1 (Transmit AIS Down-stream upon AIS), 3 (Transmit AIS Down-stream upon LOF) and 5 (Transmit AIS Down-stream upon LOS), within the "Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Primary Frame Synchronizer Block" to "1", as depicted below.

Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Primary Frame Synchronizer Block (Indirect Address = 0xNE, 0x4D; Direct Address = 0xNF4D)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	0

Q8.16: If the user has selected "Frame Generator/Frame Synchronizer Configuration # 28" can the user configure the DS3/E3 block to automatically transmit the DS3/E3 AIS indicator (in the Egress Direction) in response to the corresponding Receive SONET POH Processor block declaring the PDI-P defect condition?

A8.16: The answer to this question is "Yes". Let us presume that the corresponding Receive SONET POH Processor block has detected the PDI-P indicator, within the STS-1 signal that it is receiving from the SONET/SDH Network. If the user configured the XRT94L43 device accordingly, the DS3/E3 Frame Generator block will respond (to this detection of PDI-P) by automatically generating and transmitting the AIS signal (in the Egress Direction) for the duration that this PDI-P defect exists.

Figure 8-19 presents an illustration of the XRT94L43 device implementing this PDI-P Detection and resulting transmission of AIS scheme.

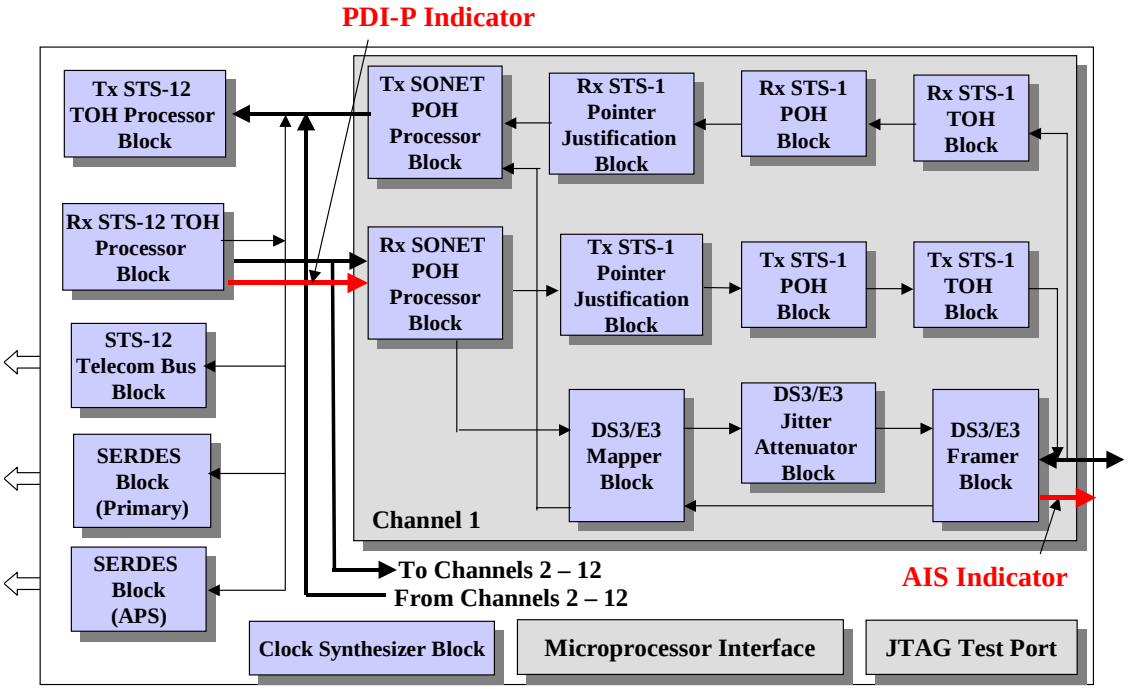

Figure 8-19 Illustration of the Receive SONET POH Processor block detecting the PDI-P condition, the resulting transmission of the AIS signal down-stream (towards the DS3/E3 LIU devices)

Implementing this PDI-P Defect/AIS Transmission Configuration

The user can configure this "PDI-P Defect detection and "automatic AIS transmission feature by setting Bit 0 (DS3 AIS upon Async PDI-P or AIS-P), within the "Receive STS-1 Path – Control Register – Byte 1", to "1" as depicted below.

Receive SONET Path – Control Register – Byte 1 (Indirect Address = 0xN0, 0x82; Direct Address = 0xN182)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused							DS3 AIS upon Async PDI-P or AIS-P
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	1

Q8.17: Does the Primary Synchronizer block (within the DS3/E3 Framer block) contain Performance Monitor registers that accumulate LCV (Line Code Violations) and EXZs (Excessive Zeros)?

A8.17: Yes, each of the twelve (12) DS3/E3 Framer blocks contains a 16-bit Performance Monitor register that is incremented anytime the Primary Frame Synchronizer block detects either LCVs (Line Code Violations) or EXZs (Excessive Zero events).

The bit-format and address location of PMON Line Code Violation Registers are presented below.

PMON Line Code Violation Count Registers – MSB (Indirect Address = 0xNE, 0x50; Direct Address = 0xNF50)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_LCV_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Line Code Violation Count Registers – LSB (Indirect Address = 0xNE, 0x51; Direct Address = 0xNF51)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_LCV_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

The bit-formation and address locations of the PMON Excessive Zero Count Registers are presented below.

PMON Excessive Zero Count Registers – MSB (Indirect Address = 0xNE, 0x4E; Direct Address = 0xNF4E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_EXZ_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Excessive Zero Count Registers – LSB (Indirect Address = 0xNE; 0x4F; Direct Address = 0xNF4F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_EXZ_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Another register that is relevant to reading out the contents of these Performance Monitor registers is the "PMON Holding" Register. The address and bit-format for these registers is presented below.

PMON Holding Register (Indirect Address = 0xNE, 0x6C; Direct Address = 0xNF6C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMON_Hold_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

THINGS TO NOTE ABOUT THESE PERFORMANCE MONITOR REGISTERS

1. Since these Performance Monitor registers count "Line-related" parameters like "Line Code Violations" and "Excessive Zeros", then it is imperative that the user select a Framer Generator/Frame Synchronizer configuration such that the Primary Synchronizer block is operating in the Ingress Path (e.g., thereby configuring the Primary Synchronizer block to receive the recovered clock and data signal from the off-chip DS3/E3/STS-1 LIU IC. (For example, Frame Generator/Frame Synchronizer Configuration # 28 is a good choice of a configuration to use).
2. The user must execute the following procedure when reading out the contents of the PMON Line Code Violation Count Registers.
    a. The user should first read out the contents of the "PMON Line Code Violation Count" Register – MSB (Indirect Address = 0xNE, 0x50; Direct Address = 0xNF50). The user will obtain the MSB (Most Significant Byte or the "Upper Byte") value of the 16-byte word expression for accumulated LCVs, during this read operation.
    b. The user should then read out the contents of the "PMON Holding" Register (Indirect Address = 0xNE, 0x6C; Direct Address = 0xNF6C). The user will obtain the LSB (Least Significant Byte or the "Lower Byte") value of the 16-byte word expression for accumulated LCVs, during this read operation.
3. The user must execute the following procedure when reading out the contents of the "PMON Excessive Zero Count" Registers

a. The user should first read out the contents of the "PMON Excessive Zero Count" Register – MSB (Indirect Address = 0xNE, 0x4E; Direct Address = 0xNF4E). The user will obtain the MSB (Most Significant Byte or the "Upper Byte" value) of the 16-byte word expression for accumulated EXZs, during this read operation.
b. The user should then read out the contents of the "PMON Holding" Register (Indirect Address = 0xNE, 0x6C; Direct Address = 0xNF6C). The user will obtain the LSB (Least Significant Byte or the "Lower Byte" value) of the 16-byte word expression for accumulated EXZs, during this read operation.

Q8.18: How should one interface a DS3/E3/STS-1 LIU IC to the XRT94L43 device in order to ensure that the Primary Synchronizer block (within the DS3/E3 Framer block) will properly increment the "LCV" or "EXZ" Performance Monitor Registers, whenever it detects LCVs or EXZs in the incoming DS3 or E3 line signal?

A8.18: The user must do all of the following things in order to properly interface the LIUs to the "low-speed" inputs of the XRT94L43 device.

1. He/she must connect the LIU to the XRT94L43 device in a manner as depicted below in Figure 8-20.

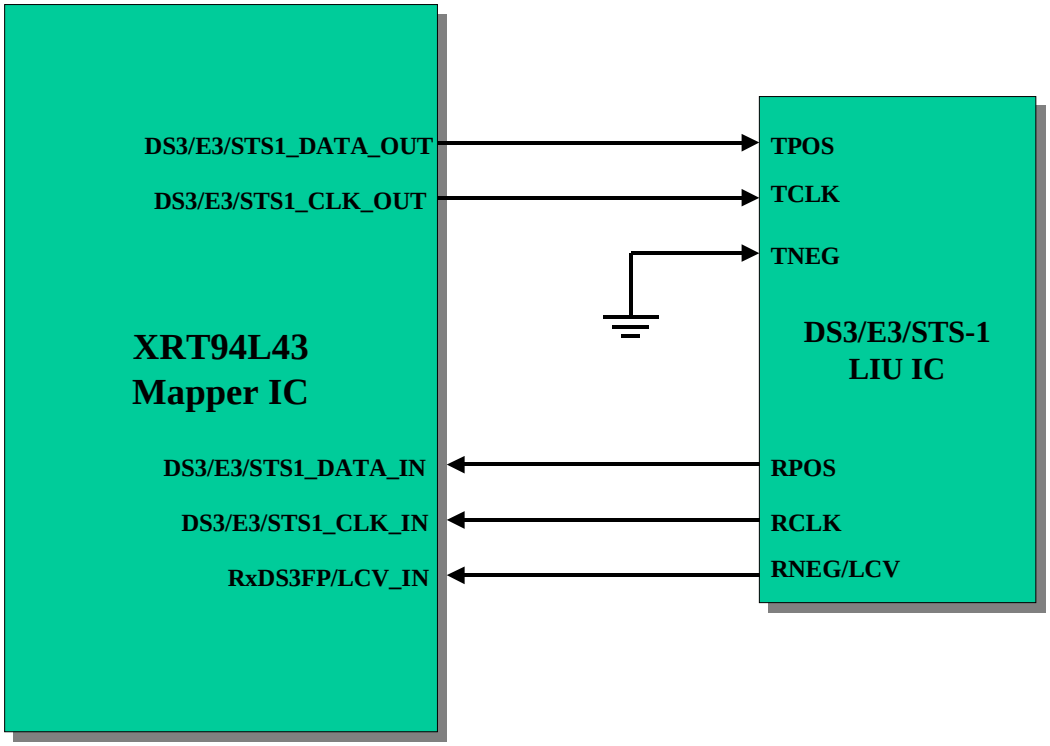

Figure 8-20, Illustration on how one should connect/interface a given DS3/E3 LIU Device to the "Low-Speed" Inputs of the XRT94L43 device

SOME NOTES ABOUT FIGURE 8-20:

The TNEG (TxNEG or TNDATA) input pins to the LIU IC must be tied to GND.

In the case of the XRT73L04 and XRT75L0X devices, the user should connect the "RNEG (RxNEG) output pin to the "RxDS3FP/LCV" input pin of the XRT94L43 device. If these particular LIU devices are configured to operate in the Single-Rail Mode, then the "RNEG" output pin then functions as the "LCV" output pin.

In the case of the XRT73L00 through XRT73L03/XRT73LC03 devices, the user should connect the dedicated "LCV" output pin to the "RxDS3FP/LCV" input pin of the XRT94L43 device.

2. He/she must select the appropriate Frame Generator/Frame Synchronizer Configuration such that the "Primary Frame Synchronizer" block is operating in the Ingress Path.

NOTES:

a. The "Primary Frame Synchronizer" block is the only entity that is capable of detecting LCVs and EXZs events.

b. Frame Generator/Frame Synchronizer Configuration # 28 is a good choice of a configuration to use. The user can implement this configuration by writing the value 0xE6 into the "Mapper Control Register" as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

c. Figure 8-21 presents an illustration of "Frame Generator/Frame Synchronizer Configuration # 28".

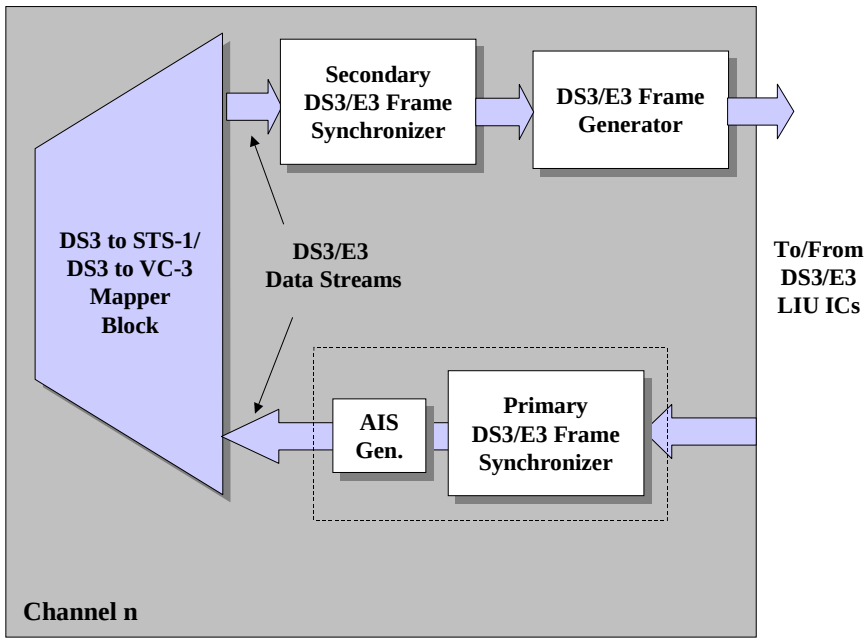

Figure 8-21, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 28".

3. Both the LIU Channels and the "DS3/E3 Framer" block (within the XRT94L43 device) must be configured to operate in the "Single-Rail" Mode. In the case of the XRT94L43 device, the can configure a given DS3/E3 Framer block to operate in the "Single-Rail" Mode by setting Bit 3 (Single-Rail/Dual-Rail) to "1" as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3/STS1 CLK OUT Invert	DS3/E3/ STS1 CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	0	0	0

Frequently Asked Questions regarding the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/STM-4 Mapper IC

Preliminary

August 15, 2006

Q8.19: Can the XRT94L43 device be configured to pass an E3, ITU-T G.751 Signal through the DS3/E3 Framer block (in both the Ingress and Egress Direction) when mapping this E3 signal into, or de-mapping this E3 signal from SDH without altering the E3 Overhead Bits?

A8.19: Yes, the DS3/E3 Framer block (within the XRT94L43 device) can be configured to "pass" an E3 signal (in both the Ingress and Egress Direction) when mapping this E3 signal into, or de-mapping this E3 from SDH, without altering the Overhead bits. The user can accomplish this by executing the following three steps.

STEP 1 – Configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer" Configuration # 0xE6.

This is accomplished by writing the value "0xE6" into the "Mapper Control Register – T3/E3 Routing Register Byte, as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xNE, 0x13; Direct Address = 0xNF13)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

NOTES:

1. The number "N" (which is used in the address location for the "Mapper Control" Register ranges from 0x01 through 0x0C for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).
2. Out of all of the Frame Generator/Frame Synchronizer configurations, this particular configuration is (by far) the most commonly used configuration. The main reason for this is that this configuration (1) permits the user to do full Performance Monitoring of the DS3/E3 signal that has been received via the Ingress Path (e.g., the LIU IC) and (2) still support the automatic transmission of the AIS indicator upon defects being declared in either direction.

Once the user executes this step, then the DS3/E3 Framer block will be operating in the "0xE6" configuration, which is presented below in Figure 8-22.

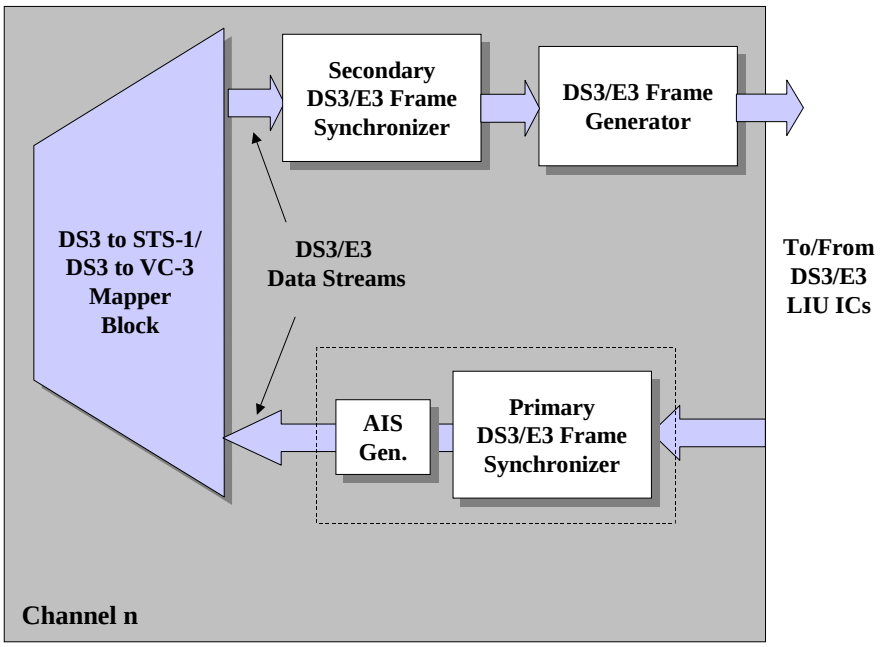

Figure 8-22, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 0xE6".

NOTE: The Primary Frame Synchronizer block does NOT alter the content of any DS3/E3 data that passes through it. Therefore, for the "0xE6 Configuration" there is no problem passing E3 data through the DS3/E3 Framer block (in the Ingress Direction) in an "un-altered" manner. We only need to take steps to prevent the DS3/E3 Frame Generator block from altering the contents of the E3 data in the Egress Direction. These remaining steps will address this concern.

STEP 2 – Configure the Frame Generator block to operate in the "Local-Timing/Frame-Slave" Mode

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Framer Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 3 – Configure the Frame Generator block to accept (and insert) the value that it receives (for the A, N and FAS bits) from the "Secondary Frame Synchronizer" block

The user can accomplish this by writing the value "0x59" into the "Transmit E3 Configuration Register – G.751" as depicted below.

Transmit E3 Configuration Register – G.751 (Indirect Address = 0xNE, 0x30; Direct Address = 0xNF30)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxBIP-4 Enable	TxASrcSel[1:0]		TxNSrcSel[1:0]		TxAIS Enable	TxLOS Enable	TxFAS Source Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	1	1	0	0	1

Q8.20 Can the XRT94L43 device be configured to pass an E3, ITU-T G.832 Signal through the DS3/E3 Framer block (in both the Ingress and Egress Direction) when mapping this E3 signal into, or de-mapping this E3 signal from SDH without altering the E3 Overhead bytes?

A8.20: Yes, the DS3/E3 Framer block (within the XRT94L43 device) can be configured to "pass" an E3 signal (in both the Ingress and Egress Direction) when mapping this E3 signal into, or de-mapping this E3 from SDH, without altering the Overhead bytes. The user can accomplish this by executing the following steps.

STEP 1 – Configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer" Configuration # 0xE6.

This is accomplished by writing the value "0xE6" into the "Mapper Control Register – T3/E3 Routing Register Byte, as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

NOTES:

1. The number "N" (which is used in the address location for the "Mapper Control" Register ranges from 0x01 through 0x0C for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).
2. Out of all of the Frame Generator/Frame Synchronizer configurations, this particular configuration is (by far) the most commonly used configuration. The main reason for this is that this configuration (1) permits the user to do full Performance Monitoring of the DS3/E3 signal that has been received via the Ingress Path (e.g., the LIU IC) and (2) still support the automatic transmission of the AIS indicator upon defects being declared in either direction.

Once the user executes this step, then the DS3/E3 Framer block will be operating in the "0xE6" configuration, which is presented below in Figure 8-23.

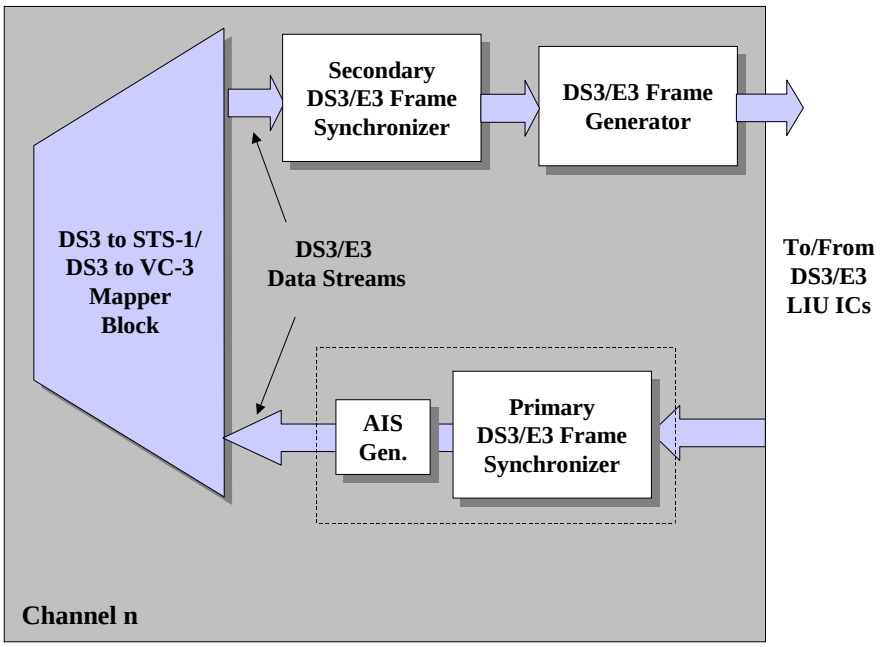

Figure 8-23, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 0xE6".

NOTE: The Primary Frame Synchronizer block does NOT alter the content of any DS3/E3 data that passes through it. Therefore, for the "0xE6 Configuration" there is no problem passing E3 data through the DS3/E3 Framer block (in the Ingress Direction) in an "un-altered" manner. We only need to take steps to prevent the DS3/E3 Frame Generator block from altering the contents of the E3 data in the Egress Direction. These remaining steps will address this concern.

STEP 2 – Configure the Frame Generator block to operate in the "Local-Timing/Frame-Slave" Mode

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Framer Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 3 – Set Bit 7 (TxOHSrc), within the "Test Register" to "1" as depicted below

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xN30C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
1	0	0	0	0	0	0	0

Once the user executes this step, then the DS3/E3 Frame Generator block will be configured to accept the overhead bits from the Secondary DS3/E3 Frame Synchronizer block, and it will insert this data into the Overhead bit-positions within the outbound E3 data-stream.

STEP 4 – Make sure that the Appropriate Set of the following (shaded) bits, within the next four registers (below) is set to "0" (the default value).

TxDS3 F-Bit Mask # 1 Register (Indirect Address = 0xNE, 0x36; Direct Address = 0xN336)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GC Byte, Bit 7	GC Byte, Bit 6	GC Byte, Bit 5	GC Byte, Bit 4	GC Byte, Bit 3	GC Byte, Bit 2	GC Byte, Bit 1	GC Byte, Bit 0
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TxDS3 F-Bit Mask # 2 Register (Indirect Address = 0xNE, 0x37; Direct Address = 0xN337)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NR Byte, Bit 7	NR Byte, Bit 6	NR Byte, Bit 5	NR Byte, Bit 4	NR Byte, Bit 3	NR Byte, Bit 2	NR Byte, Bit 1	NR Byte, Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TxDS3 F-Bit Mask # 3 Register (Indirect Address = 0xNE, 0x38; Direct Address = 0xN338)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MA Byte, Bit 7 (FERF)	MA Byte, Bit 6 (FEBE)	MA Byte, Bit 5	MA Byte, Bit 4	MA Byte, Bit 3	MA Byte, Bit 2	MA Byte, Bit 1	MA Byte, Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

TxDS3 F-Bit Mask # 4 Register (Indirect Address = 0xNE, 0x39; Direct Address = 0xNF39)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TR Byte, Bit 7	TR Byte, Bit 6	TR Byte, Bit 5	TR Byte, Bit 4	TR Byte, Bit 3	TR Byte, Bit 2	TR Byte, Bit 1	TR Byte, Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This step configures the "DS3/E3 Frame Generator" block to accept the overhead data (from the Secondary DS3/E3 Frame Synchronizer" block) for these particular bit-fields, and to insert this data into the overhead bit-fields (A and N-bit positions) within the outbound E3 data-stream.

NOTE: If any of these bit-fields are set to "1", then the "DS3/E3 Frame Generator" block will NOT accept nor insert the overhead data (from the Secondary DS3/E3 Frame Synchronizer" block) into the overhead bit-positions that corresponds with that or those particular register bits.

Q8.21: Can one configure the XRT94L43 device to handle E3-rate data in an unframed manner?

A8.21: Yes, the DS3/E3 Framer block (within the XRT94L43 device) can be configured to "pass" an unframed E3 signal (in both the Ingress and Egress Direction) when mapping this E3 signal into, or de-mapping this E3 from SDH. The user can accomplish this by executing the following steps.

STEP 1 – Configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer" Configuration # 0xE6.

This is accomplished by writing the value "0xE6" into the "Mapper Control Register – T3/E3 Routing Register Byte, as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

NOTES:

Out of all of the Frame Generator/Frame Synchronizer configurations, this particular configuration is (by far) the most commonly used configuration. The main reason for this is that this configuration (1) permits the user to do full Performance Monitoring of the DS3/E3 signal that has been received via the Ingress Path (e.g., the LIU IC) and (2) still support the automatic transmission of the AIS indicator upon defects being declared in either direction.

Once the user executes this step, then the DS3/E3 Framer block will be operating in the "0xE6" configuration, which is presented below in Figure 8-24.

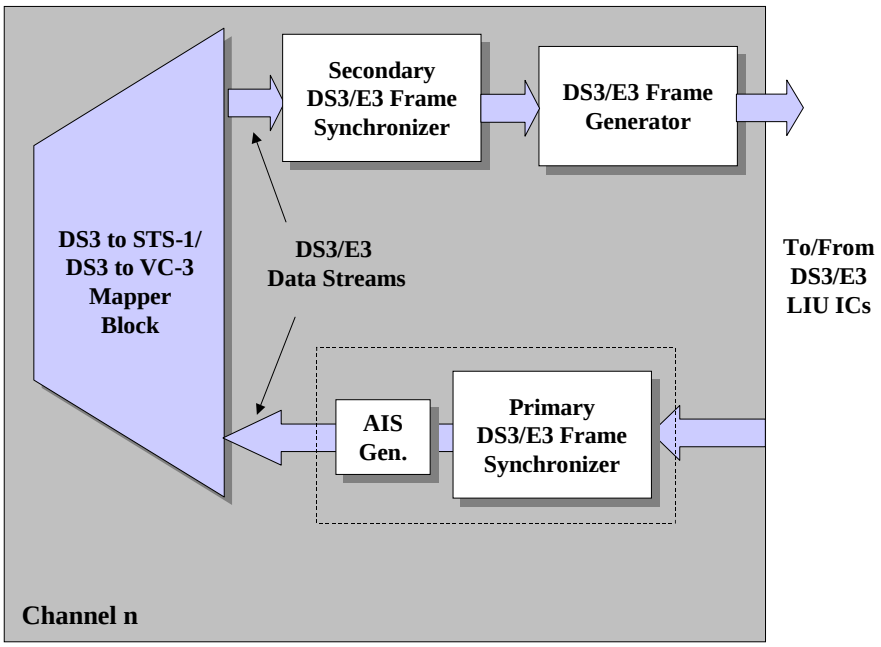

Figure 8-24, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 0xE6".

NOTE: The Primary Frame Synchronizer block does NOT alter the content of any DS3/E3 data that passes through it. Therefore, for the "0xE6 Configuration" there is no problem passing E3 data through the DS3/E3 Framer block (in the Ingress Direction) in an "un-altered" manner. We only need to take steps to prevent the DS3/E3 Frame Generator block from altering the contents of the E3 data in the Egress Direction. These remaining steps will address this concern.

STEP 2 – Configure the Frame Generator block to operate in the "Local-Timing/Frame-Slave" Mode

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Framer Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 3 – Configure the Frame Generator block to accept (and insert) the value that it receives (for the A, N and FAS bits) from the "Secondary Frame Synchronizer" block

This step will (in affect) by-pass the Frame Generator block. The user can accomplish this by writing the value "0x59" into the "Transmit E3 Configuration Register – G.751" as depicted below.

Transmit E3 Configuration Register – G.751 (Indirect Address = 0xNE, 0x30; Direct Address = 0xNF30)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxBIP-4 Enable	TxASrcSel[1:0]		TxNSrcSel[1:0]		TxAIS Enable	TxLOS Enable	TxFAS Source Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	1	1	0	0	1

Q8.22: Can one configure the XRT94L43 device to handle DS3-rate data in an unframed manner?

A8.22: Yes, the DS3/E3 Framer block (within the XRT94L43 device) can be configured to "pass" an unframed DS3 signal (in both the Ingress and Egress Direction) when mapping this DS3 signal into, or de-mapping this DS3 from SONET/SDH. The user can accomplish this by executing the following steps.

STEP 1 – Configure the DS3/E3 Framer block to operate in "Frame Generator/Frame Synchronizer" Configuration # 0xE6.

This is accomplished by writing the value "0xE6" into the "Mapper Control Register – T3/E3 Routing Register Byte, as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

NOTES:

1. The number "N" (which is used in the address location for the "Mapper Control" Register ranges from 0x01 to 0x0C for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).
2. Out of all of the Frame Generator/Frame Synchronizer configurations, this particular configuration is (by far) the most commonly used configuration. The main reason for this is that this configuration (1) permits the user to do full Performance Monitoring of the DS3/E3 signal that has been received via the Ingress Path (e.g., the LIU IC) and (2) still support the automatic transmission of the AIS indicator upon defects being declared in either direction.

Once the user executes this step, then the DS3/E3 Framer block will be operating in the "0xE6" configuration, which is presented below in Figure 8-25.

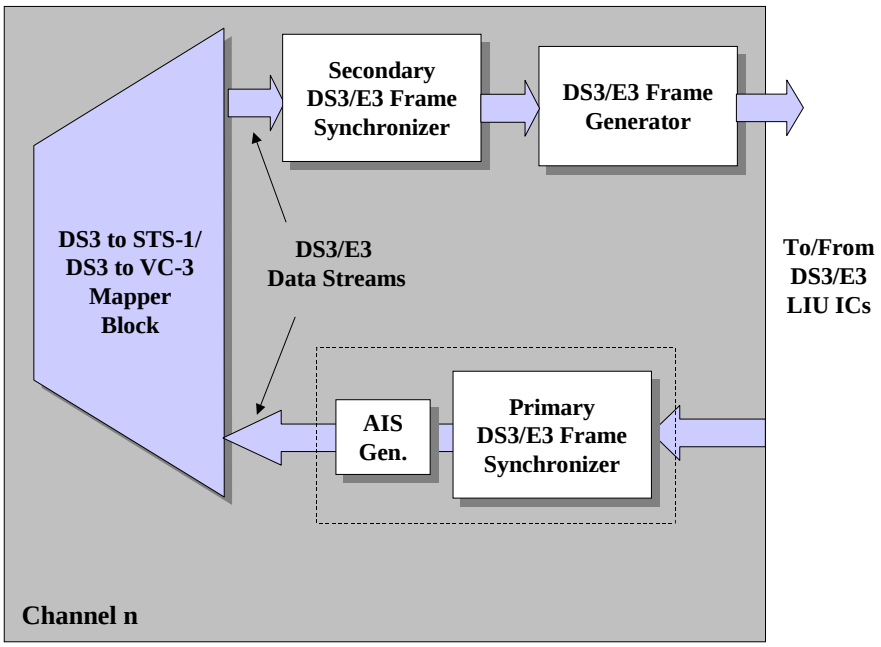

Figure 8-25, An Illustration of "Frame Generator/Frame Synchronizer Configuration # 0xE6".

NOTE: The Primary Frame Synchronizer block does NOT alter the content of any DS3/E3 data that passes through it. Therefore, for the "0xE6 Configuration" there is no problem passing DS3 data through the DS3/E3 Framer block (in the Ingress Direction) in an "un-altered" manner. We only need to take steps to prevent the DS3/E3 Frame Generator block from altering the contents of the DS3 data in the Egress Direction. These remaining steps will address this concern.

STEP 2 – Configure the Frame Generator block to operate in the "Local-Timing/Frame-Slave" Mode

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Framer Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 3 – By-pass the "Frame Generator" block.

This is accomplished by setting Bits 1 and 0 (Frame Generator Block By-Pass), within the "Test Register" to "[1, 1]", as depicted below.

Test Register (Indirect Address = 0xNE, 0x0C; Direct Address = 0xNF0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Frame Generator Block By-Pass	
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

Q9: Transmit and Receive STS-1 TOH/POH Processor Block Related Questions

Q9.1: Can the XRT94L43 device be configured to process STS-1 signals with VT-mapped SPEs?

A9.1: Yes, however the user will have to enable either the "POH Pass-Thru" and/or the "STS-1 POH Pass-Thru" Modes within the STS-1 channel that is handling these VT-mapped SPEs.

THE ISSUE ASSOCIATED WITH VT-MAPPED STS-1 SPEs

As VT-mapped STS-1 SPEs are created, they are created in the form of a 500µs "Super-frame" structure (which consists of four VT-mapped STS-1 SPEs). The current phase (within this 500µs "Super-Frame" structure) can be found within the H4 byte, within the STS-1 POH. It is imperative that a given PTE (which has the responsibility of de-mapping data from these VT-mapped STS-1 SPEs) know which phase (within this 500µs "Super-Frame" structure) that a given incoming STS-1 SPE is in. If the PTE "knows" this information then it can identify the VT-pointer bytes (V1, V2 and V3) within the STS-1 SPE; and, in-turn, locate the VT SPE within the STS-1 SPE.

If the PTE were to lose track of this "500µs – Super-frame" phase information, then the PTE would declare the LOP-V condition and would not be able to properly extract out the data that has been VT-mapped into the STS-1 SPE.

In order to thoroughly understand the material below, the reader is advised to refer to the Functional Block Diagram of the XRT94L43 device, below in Figure 9-1.

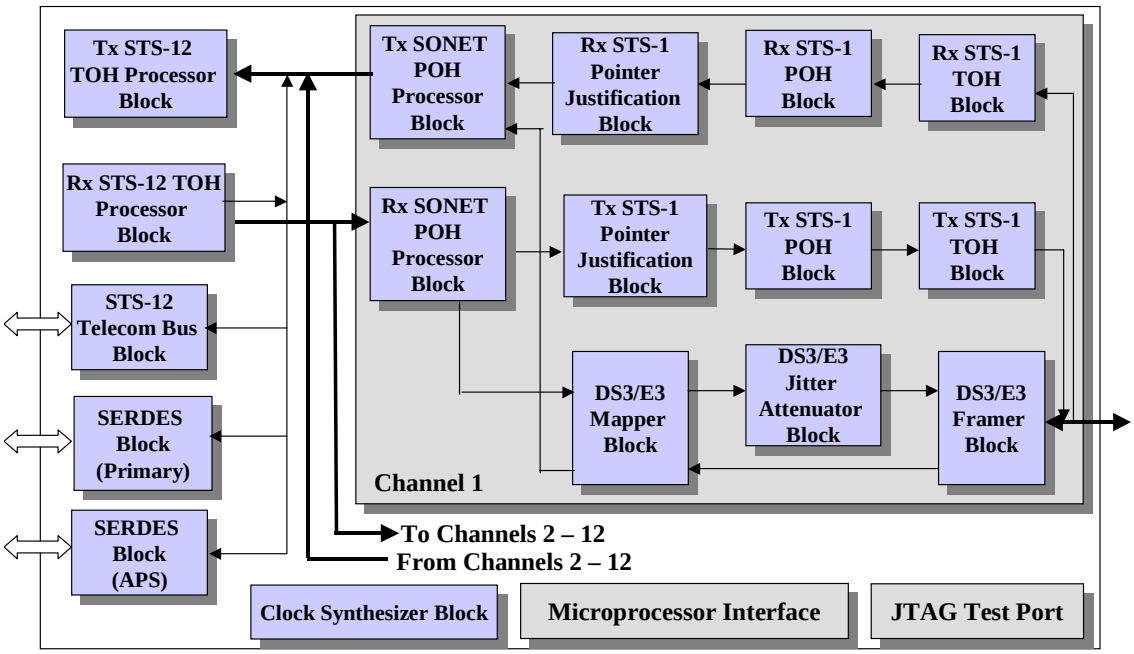

Figure 9-1, Illustration of the Functional Block Diagram of the XRT94L43 Device

If the user applies a VT-mapped STS-1 data-stream to any one of the twelve (12) Receive STS-1 inputs (within the XRT94L43 device), then the following events will occur.

a. The Receive STS-1 TOH Processor block will receive this STS-1 signal, terminate and process the TOH data and it will pass the resulting STS-1 SPE to the Receive STS-1 POH Processor block for further processing.
b. The Receive STS-1 POH Processor block will receive this STS-1 SPE signal, and will terminate and process the POH data. Afterwards, the STS-1 SPE data will be routed to the Transmit SONET POH Processor block, for further processing.
c. The Transmit SONET POH Processor block will receive this particular STS-1 SPE, and it will re-compute and insert the entire POH data (including a new H4 byte value) into this particular STS-1 SPE, prior to routing this data to the Transmit STS-12 TOH Processor block.

NOTE: In this mode, the Transmit SONET POH Processor block will NOT be using the POH data (received by the Receive STS-1 POH Processor block) as the source for the H4 byte, in each "outbound" STS-1 data-stream. Instead, the Transmit SONET POH Processor block will either use the contents of the "Transmit SONET – Transmit H4 Byte" Register, or data that has been inserted via the "TxPOH" input port, as the source for the H4 byte.

As a consequence, this "500µs – Super-frame" signaling information (that was provided within the H4 byte) is now "wiped-out" and will be unavailable to the remote PTE as it attempts to de-map and extract data out of its incoming VT-Mapped STS-1 SPEs.

Similarly, if the user were to apply an STS-12 signal to either the Receive STS-12/STM-4 PECL Interface or the Receive STS-12/STM-4 Telecom Bus Interface; that just happens to contain a VT-mapped STS-1 signal, then the following events will occur.

a. The Receive STS-12 TOH Processor block will receive this STS-12 signal, terminate and process the TOH data, and will then byte de-interleave this STS-12 signal into up to twelve (12) STS-1 signals. Each of these STS-1 signals are then routed to their corresponding Receive SONET POH Processor blocks for further processing.
b. The Receive SONET POH Processor block will receive this STS-1 SPE signal, and will terminate and process the POH data. Afterwards, the STS-1 SPE data will be routed to the Transmit STS-1 POH Processor block, for further processing.
c. The Transmit STS-1 POH Processor block will receive this particular STS-1 SPE, and it will re-compute and insert the entire POH data (including a new H4 byte value) into this particular STS-1 SPE, prior to routing this data to the Transmit STS-1 TOH Processor block.

NOTE: In this mode, the Transmit STS-1 POH Processor block will NOT be using the POH (received by the Receive SONET POH Processor block) as the source for the H4 byte, in each "outbound" STS-1 data-stream. Instead, the Transmit STS-1 POH Processor block will either use the contents of the "Transmit STS-1 Transport – Transmit H4 Byte" register, or data that has been inserted via the "TxPOH" input port, as the source for the H4 byte.

As a consequence, this "500µs – Super-frame" signaling information (that was provided within the H4 byte) is now "wiped-out" and will be unavailable to the remote PTE as it attempts to de-map and extract data out of its incoming VT-Mapped STS-1 SPEs.

HOW TO GET AROUND THIS PROBLEM

The XRT94L43 supports both the "POH Pass-Thru" and the "STS-1 POH Pass-Thru" of operation. Each of these modes of operation is described below.

The "POH Pass-Thru" Mode

In the "POH Pass-Thru" Mode, the "POH Computation and Insertion" feature of the Transmit SONET POH Processor block will be disabled; and the POH data (residing within each STS-1 SPE) that is received by the Receive STS-1 POH Processor block will pass through to the Transmit STS-12 TOH Processor block without modification. In other words, in the "POH Pass-Thru" Mode, the POH within an STS-1 SPE (which is traveling from one of the Receive STS-1 inputs to the Transmit STS-12 outputs) will pass-thru without modification.

The user can configure a given channel to operate in the "POH Pass-Thru" Mode by setting Bit 2 (POH Pass-Thru), within the "Mapper Control Register – Byte 2" to "1" as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

Figure 9-2 presents an illustration of a given Channel (within the XRT94L43 device) operating in the POH Pass-Thru Mode.

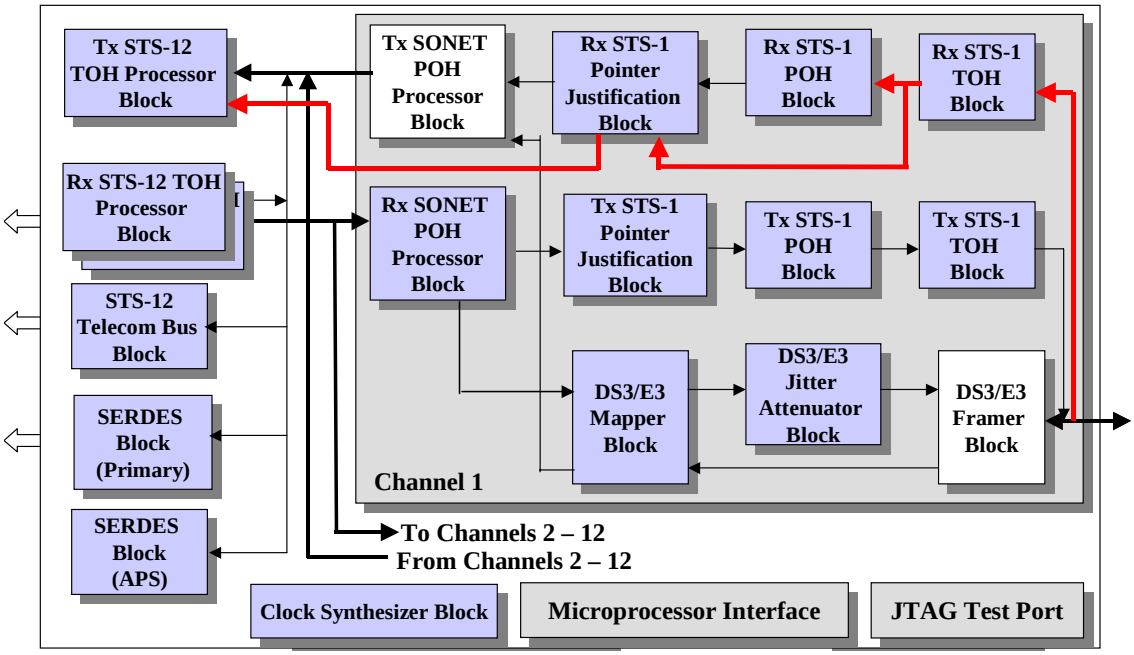

Figure 9-2, Illustration of a Given Channel (within the XRT94L43 device) operating in the POH Pass-Thru Mode.

The "STS-1 POH Pass-Thru" Mode

In the "STS-1 POH Pass-Thru" Mode, the "POH Computation and Insertion" feature of the Transmit STS-1 POH Processor block will be disabled; and the POH data (residing within each STS-1 SPE) that is received by the Receive SONET POH Processor block will pass through to the Transmit STS-1 TOH Processor block without modification. In other words, in the "STS-1 POH Pass-Thru" Mode, the POH within an STS-1 SPE (which is traveling from the Receive STS-12/STM-4 PECL Interface" or "Telecom Bus Interface" to one of the Transmit STS-1 outputs) will pass-thru without modification.

The user can configure a given channel to operate in the "STS-1 POH Pass Thru" Mode by setting Bit 7 (STS-1 POH Pass Thru), within the "Mapper Control Register – Byte 2" to "1" as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

Figure 9-3 presents an illustration of a given Channel (within the XRT94L43 device) operating in the STS-1 POH Pass-Thru Mode.

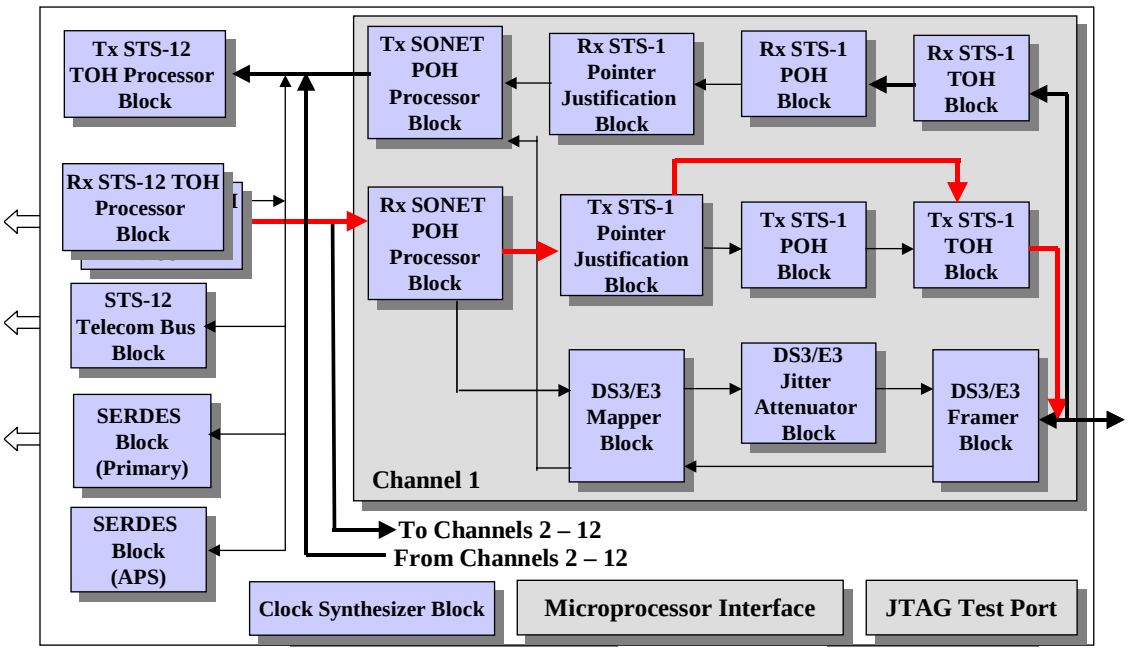

Figure 9-3, Illustration of a Given Channel (within the XRT94L43 device) operating in the STS-1 POH Pass-Thru Mode.

Q9.2: Does the XRT94L43 device permit the user to control the values of certain TOH bytes, within the 12 outbound STS-1 signals, via on-chip registers?

A9.2: Yes, the circuitry associated with each of the 12 Transmit STS-1 TOH Processor blocks (within the XRT94L43 device) permit the user to control all of the following TOH bytes via on-chip registers.

- K1
- K2
- M0
- S1
- F1
- E1
- E2
- J0

The on-chip registers associated with each of these TOH bytes are presented below.

For the K1 Byte:

Transmit STS-1 Transport – K1K2 (APS) Value Register – Byte 1 (Indirect Address = 0xNA, 0x2F; Direct Address = 0xNB2F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_K1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the K2 Byte:

Transmit STS-1 Transport – K1K2 (APS) Value Register – Byte 1 (Indirect Address = 0xNA, 0x2E; Direct Address = 0xNB2E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_K2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the M0 Byte:

Transmit STS-1 Transport – M0M1 Value Register (Indirect Address = 0xNA, 0x37; Direct Address = 0xNB37)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_M0M1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the S1 Byte:

Transmit STS-1 Transport – S1 Byte Value Register (Indirect Address = 0xNA, 0x3B; Direct Address = 0xNB3B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_S1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the F1 Byte:

Transmit STS-1 Transport – F1 Byte Value Register (Indirect Address = 0xNA, 0x3F; Direct Address = 0xNB3F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_F1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the E1 Byte:

Transmit STS-1 Transport – E1 Byte Value Register (Indirect Address = 0xNA, 0x43; Direct Address = 0xNB43)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_E1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the E2 Byte:

Transmit STS-1 Transport – E2 Byte Value Register (Indirect Address = 0xNA, 0x47; Direct Address = 0xNB47)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_E2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the J0 Byte:

Transmit STS-1 Transport – J0 Byte Value Register (Indirect Address = 0xNA, 0x4B; Direct Address = 0xNB4B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_J0_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The Transmit STS-1 Transport – J0 Byte Value Register should only be used if the user has selected a "Section Trace Message" size of 1 byte.

Looking at this another way:
The TOH bytes, that the Transmit STS-1 TOH Processor block permits the user to have software (on-chip) register control over their contents, are designated by the "highlighted" bytes within Figure 9-4 below.

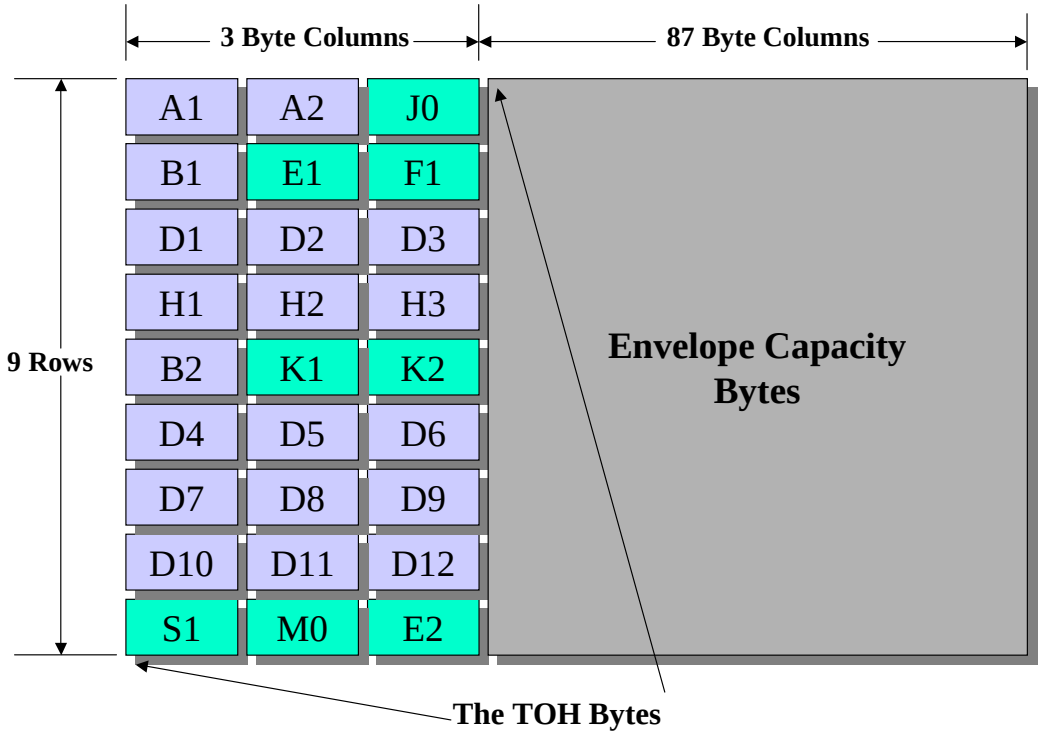

Figure 9-4, Illustration of the STS-1 frame, with the "TOH Bytes" whose contents can be controlled (by the Transmit STS-1 TOH Processor block), via "on-chip" registers are designated

Q9.3: Does the XRT94L43 device permit the user to monitor the values of certain TOH bytes by software (via on-chip registers), within the 12 inbound STS-1 signals, via on-chip registers?

A9.3: Yes, the circuitry associated with each of the 12 Receive STS-1 TOH Processor blocks (within the XRT94L43 device) permits the user to monitor the values of all of the following TOH bytes (within the incoming STS-1 data-stream) via on-chip registers.

- K1
- K2
- S1
- J0*

The on-chip registers associated with each of these TOH bytes are presented below.

For the K1 Byte:

Receive STS-1 Transport – Received K1 Byte Value (Indirect Address = 0xN2, 0x1F; Direct Address = 0xN31F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Filtered_K1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the K2 Byte:

Receive STS-1Transport – Received K2 Byte Value (Indirect Address = 0xN2, 0x23; Direct Address = 0xN323)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Filtered_K2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the S1 Byte:

Receive STS-1 Transport – Received S1 Byte Value (Indirect Address = 0xN2, 0x27; Direct Address = 0xN327)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Filtered_S1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the J0 Byte:

NOTE: In the case of the J0 byte, the user can read obtain the contents of the entire, most recently received Section Trace Message, (which is transported by the J0 byte) by reading out the contents of the "Receive Section Trace" Buffer for the Receive STS-1 TOH Processor block. The steps on how to read out the contents of the "Receive Section Trace" Buffer, associated with a given Receive STS-1 TOH Processor block is presented below in Question Q9.4.

Looking at this another way:

The TOH bytes, that the Receive STS-1 TOH Processor block permits the user to monitor via software (on-chip) registers, are designated by the "highlighted" bytes within Figure 9-5, below.

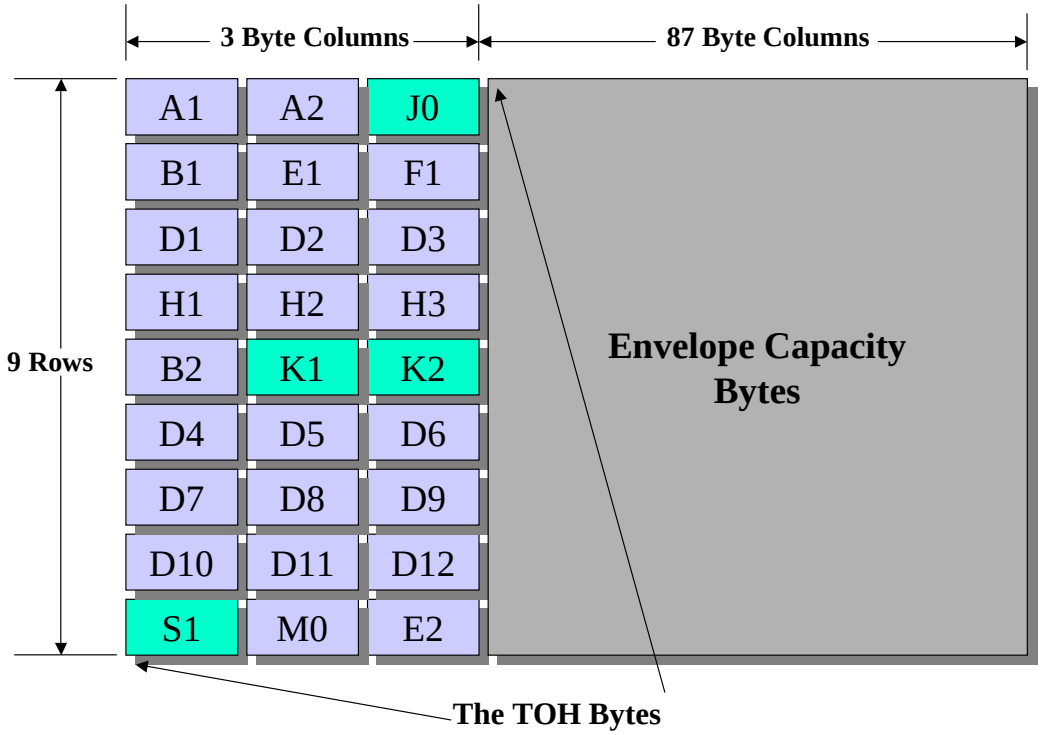

Figure 9-5, Illustration of the STS-1 frame, with the "TOH Bytes" whose contents can be monitored (by the Receive STS-1 TOH Processor block), via "on-chip" registers are designated

SOME IMPORTANT CAVIOTS ASSOCIATED WITH THIS PARTICULAR QUESTION:

If the user wishes to execute the "above-mentioned" steps, in order to obtain the contents of these various TOH bytes, within the most recently received STS-1 frame, then he/she must be aware of the following.

1. All of the address locations (for each of these Registers) are expressed in terms of "0xN2, 0xMM" or "0xN3MM". This case the value "N" corresponds with the channel number (of the Receive STS-1 TOH Processor block), and can range in value of 1 (for Channel 0) to C (for Channel 11).
2. Prior to executing any read operations from the "above-mentioned" registers, the user must ensure that Bits 1 and 0 (STS-1 Access_SEL[1:0]) within the "Mode Control Register – Byte 1" is set to the values of "[0, 0]", as depicted below.

Mode Control Register – Byte 1 (Indirect = 0x00, 0x1A; Direct Address = 0x011A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						STS-1 Access_SEL[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

By ensuring this configuration setting, the user will be accessing the "Receive STS-1 TOH Processor Block" control registers (in lieu of the Section or Path Trace Message Buffers), anytime the Microprocessor performs a READ or WRITE operation to address locations "0xN300 through 0xN33F".

Q9.4: What procedure must one execute in order to read out the contents of the most recently received Section Trace Message, within a given STS-1 signal, that is being received by a given Receive STS-1 TOH Processor block?

A9.4: The user can read out the contents of the most recently received "Section Trace" Message from the "Receive STS-1 Section Trace" Message Buffer, by executing the following steps.

STEP 1- Write the value "0x01" into the "Mode Control Register – Byte 1" as depicted below.

Mode Control Register – Byte 1 (Indirect = 0x00, 0x1A; Direct Address = 0x011A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						STS-1 Access_SEL[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	1

This step will configure the XRT94L43 device to access either the "Receive STS-1" Section Trace Message – Expected Value Message" Buffer or the "Receive STS-1 Section Trace Message - Actual Received Message" Buffer anytime a read operation is performed within the address range of "0xN300 through 0xN33F".

STEP 2 – Set Bit 4 (READ_SEL), within the "Receive STS-1 Transport – Receive J0 Trace Buffer Control Register", to "0" as depicted below.

Receive STS-1 Transport – Receive J0 Trace Buffer Control Register (Indirect Address = 0xN2, 0x4F; Direct Address = 0xN34F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused			READ SEL	ACCEPT THRD	MSG TYPE	MSG LENGTH	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	X	X	X	X

This step configures the XRT94L43 device to output the contents of the "Receive STS-1 Section Trace – Actual Received Message" Buffer, anytime a read operation is performed within the address range of "0xN300 through 0xN33F".

STEP 3 – Begin to read out the appropriate number of bytes from the "Receive STS-1 Section Trace – Actual Message" buffer.

In this case, the first byte within this buffer will reside in address location 0xN300. The remainder of the text below provides the user with instructions on reading out the contents of the "Most Recently Received" Section Trace Message, as a function of "Message Size".

If the Section Trace Message Size = 1 Byte

If the size of the "Section Trace" Message is configured to be 1 byte, then the user will have completed the task of reading out the entire contents of the "Section Trace" Message by reading out the contents of address location 0xN300.

If the Section Trace Message Size = 16 bytes

If the Section Trace Message Size is 16 bytes, then the user must read out the contents of address locations 0xN300 through 0xN30F. Once the user has executed these 16 READ operations then he/she will have completed the task of reading out the entire contents of the "Section Trace" Message.

If the Section Trace Message Size = 64 bytes

If the Section Trace Message Size is 64 bytes, then the user must read out the contents of address locations 0xN300 through 0xN33F. Once the user has executed these 64 READ operations then he/she will have completed the task of reading out the entire contents of the "Section Trace" Message.

Q9.5: What procedure must one execute in order to read out the contents of the most recently received Path Trace Message, within a given STS-1 signal, that is being received by a given Receive STS-1 POH Processor block?

A9.5: The user can read out the contents of the most recently received "Path Trace" Message from the "Receive STS-1 Path Trace" Message Buffer, by executing the following steps.

STEP 1 – Write the value "0x02" into the "Mode Control Register – Byte 1" as depicted below.

Mode Control Register – Byte 1 (Indirect = 0x00, 0x1A; Direct Address = 0x011A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						STS-1 Access_SEL[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	1	0

This step will configure the XRT94L43 device to access either the "Receive STS-1 Path Trace Message – Expected Value Message" Buffer of the "Receive STS-1 Path Trace Message – Actual Received Message" Buffer anytime a read operation is performed within the address range of "0xN300 through 0xN33F".

STEP 2 – Set Bit 4 (Receive J1 Message Buffer Read Select), within the "Receive STS-1 Path – Receive J1 Control Register", to "0" as depicted below.

Receive STS-1 Path – Receive J1 Control Register (Indirect Address = 0xN2, 0xA3; Direct Address = 0xN3A3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused			Receive J1 Message Buffer Read Select	Accept Threshold	Message Type	Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This step configures the XRT94L43 device to output the contents of the "Receive STS-1 Path Trace – Actual Received Message" Buffer, anytime a read operation is performed within the address range of "0xN300 through 0xN33F".

STEP 3 – Begin to read out the appropriate number of bytes from the "Receive STS-1 Path Trace – Actual Message" buffer.

In this case, the first byte within this buffer will reside in address location 0xN300. The remainder of the text below provides the user with instructions on reading out the contents of the "Most Recently Received" Path Trace Message, as a function of "Message Size".

If the Path Trace Message Size = 1 Byte

If the size of the "Path Trace" Message is configured to be 1 byte, then the user will have completed the task of reading out the entire contents of the "Path Trace" Message by reading out the contents of address location 0xN300.

If the Path Trace Message Size = 16 bytes

If the Path Trace Message Size is 16 bytes, then the user must read out the contents of address locations 0xN300 through 0xN30F. Once the user has executed these 16 READ operations then he/she will have completed the task of reading out the entire contents of the "Path Trace" Message.

If the Path Trace Message Size = 64 bytes

If the Path Trace Message Size is 64 bytes, then the user must read out the contents of address locations 0xN300 through 0xN33F. Once the user has executed these 64 READ operations, then he/she will have completed the task of reading out the entire contents of the "Path Trace" Message.

Q9.6: Does the XRT94L43 device permit the user to control the values of certain POH bytes, within the 12 outbound STS-1 signals, via on-chip registers?

A9.6: Yes, the circuitry associated with each of the 12 Transmit STS-1 POH Processor blocks (within the XRT94L43 device) permits the user to control all of the following POH bytes via on-chip registers.

- J1
- C2
- G1
- F2
- H4
- Z3
- Z4
- Z5

The on-chip registers associated with each of these POH bytes are presented below.

For the J1 Byte:

Transmit STS-1 Path – Transmitter J1 Byte Value Register (Indirect Address = 0xNA, 0x93; Direct Address = 0xNB93)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_J1_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The Transmit STS-1 Path – Transmitter J1 Byte Value Register should only be used if the user has selected a "Path Trace Message" size of 1 byte.

For the C2 Byte:

Transmit STS-1 Path – Transmit C2 Byte Value Register (Indirect Address = 0xNA, 0x9F; Direct Address = 0xNB9B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the G1 Byte:

Transmit STS-1 Path – Transmit G1 Byte Value Register (Indirect Address = 0xNA, 0x9F; Direct Address = 0xNB9F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the F2 Byte:

Transmit STS-1 Path – Transmit F2 Byte Value Register (Indirect Address = 0xNA, 0xA3; Direct Address = 0xNBA3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the H4 Byte:

Transmit STS-1 Path – Transmit H4 Byte Value Register (Indirect Address = 0xNA, 0xA7; Direct Address = 0xNBA7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the Z3 Byte:

Transmit STS-1 Path – Transmit Z3 Byte Value Register (Indirect Address = 0xNA, 0xAB; Direct Address = 0xNBAB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the Z4 Byte:

Transmit STS-1 Path – Transmit Z4 Byte Value Register (Indirect Address = 0xNA, 0xAF; Direct Address = 0xNBAF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the Z5 Byte:

Transmit STS-1 Path – Transmit Z5 Byte Value Register (Indirect Address = 0xNA, 0xB3; Direct Address = 0xNBB3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Q9.7: Does the XRT94L43 device permit the user to monitor the values of certain POH bytes by software (via on-chip registers), within the 12 inbound STS-1 signal that have been received via the Receive STS-1 POH Processor blocks?

A9.7: Yes, the circuitry associated with each of the 12 Receive STS-1 POH Processor blocks (within the XRT94L43 device) permits the user to monitor the values of all of the POH bytes (within the incoming STS-1 data-stream) via on-chip registers.

The on-chip registers associated with each of these POH bytes are presented below.

For the J1 Byte:

Receive STS-1 Path – Receive J1 Byte Capture Register (Indirect Address = 0xN2, 0xD3; Direct Address = 0xN3D3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the B3 Byte:

Receive STS-1 Path – Receive B3 Byte Capture Register (Indirect Address = 0xN2, 0xD7; Direct Address = 0xN3D7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the C2 Byte:

Receive STS-1 Path – Receive C2 Byte Capture Register (Indirect Address = 0xN2, 0xDB; Direct Address = 0xN3DB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the G1 Byte:

Receive STS-1 Path – Receive G1 Byte Capture Register (Indirect Address = 0xN2, 0xDF; Direct Address = 0xN3DF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the F2 Byte:

Receive STS-1 Path – Receive F2 Byte Capture Register (Indirect Address = 0xN2, 0xE3; Direct Address =0xN3E3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the H4 Byte:

Receive STS-1 Path – Receive H4 Byte Capture Register (Indirect Address = 0xN2, 0xE7; Direct Address = 0xN3E7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the Z3 Byte:

Receive STS-1 Path – Receive Z3 Byte Capture Register (Indirect Address = 0xN2, 0xEB; Direct Address = 0xN3EB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the Z4 Byte:

Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register (Indirect Address = 0xN2, 0xEF; Direct Address = 0xN3EF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

For the Z5 Byte:

Receive STS-1 Path – Receive Z5 Byte Capture Register (Indirect Address = 0xN2, 0xF3; Direct Address = 0xN3F3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Q10: Power Consumption/Thermal-Related Questions

Q10.1: What is the Power Consumption of the XRT94L43 device?

A10.1: The 2.5V and the 3.3V Current Draw for the XRT94L43, when the "Power Save" feature is disabled is as listed in Table 10-1, below.

Table 10-1, Power Consumption Information of the XRT94L43 device (when the Power Save Feature is Disabled)

Item	Current Draw	Power Consumption
2.5V Power Supply Current	1.234A	3.09W
3.3V Power Supply Current	613mA	2.02W
Total Power Consumption		**5.11W**

Table 10-2, Power Consumption Information of the XRT94L43 device (when the Power Save Feature is Enabled)

Item	Current Draw	Power Consumption
2.5V Power Supply Current	1.080A	2.70W
3.3V Power Supply Current	590mA	1.95W
Total Power Consumption		**4.65W**

Q10.2: What is the estimated Die Temperature of the XRT94L43 device?

A10.2: The XRT94L43 device comes in a 516 pin PBGA package. Therefore, the following THETA-JA values (for their corresponding conditions) apply.

Table 10-3, THETA-JA Values for a given set of Ambient Conditions

Ambient Condition	THETA-JA Value (°C/W)
Still Air, No Fin-Type Heat Sink	12.8
200 Linear feet/minute of Air Flow, with Fin-Type Heat Sink	7.8

Based upon these THETA-JA values, Table 10-4 presents the resulting Die Temperature for a variety of conditions.

Table 10-4, Resulting XRT94L43 Die Temperature for a given set of "Power Save Feature" settings and Ambient Conditions

Power Save Feature Enable/Disable Setting	Ambient Temperature	Ambient Condition	Resulting Die Temperature
Enabled	+25°C	Still Air, No Fin-Type Heat Sink	+84.5°C
Enabled	+85°C	Still Air, No Fin-Type Heat Sink	+144.5°C
Enabled	+25°C	200 Linear Feet/Minute of Air Flow, with Fin-Type Heat Sink	+61.3°C
Enabled	+85°C	200 Linear Feet/Minute of Air Flow, with Fin-Type Heat Sink	+121.3°C
Disabled	+25°C	Still Air, No Fin-Type Heat Sink	+90.4°C
Disabled	+85°C	Still Air, No Fin-Type Heat Sink	+150.4°C
Disabled	+25°C	200 Linear Feet/Minute of Air Flow, with Fin-Type Heat Sink	+64.9°C
Disabled	+85°C	200 Linear Feet/Minute of Air Flow, with Fin-Type Heat Sink	+124.9°C

NOTES:

1. The "Resulting Die Temperature" values are based upon multiplying the THETA-JA value by the Power Consumption value. This is conservative in the sense that the actual Power Dissipation (for the 3.3V power supply current) is less than the Power Consumption.
2. Based upon this information, we highly recommend that the user mount a "Fin-Type" Heat Sink on top of the package of this device, and insure that sufficient air flow will be provided (via system fans) to vicinity of the XRT94L43 package.

Q10.3: What make/model of Heat Sink should one use with the XRT94L43 device?

A10.3: Either of the following Heat Sink is acceptable.

- Wakefield 630-25AB, or
- Wakefield 642-25AB

Q11: DS3/E3/STS-1 LIU Interface Related Questions

Q11.1: Can the DS3/E3 LIU Interface of the XRT94L43 device be configured to operate in the Single-Rail Mode?

A11.1: Yes, the DS3/E3 LIU Interfaces (within the XRT94L43 device) can be configured to operate in either the Single-Rail or Dual-Rail Modes. However, the exact steps one should take in order to configure a given channel to operate in this mode depend upon whether the channel has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 23 or # 28. The procedure for configuring a given channel to operate in the Single-Rail Mode, will be provided below for both of these popular Frame Generator/Frame Synchronizer Configurations.

If the DS3/E3 Framer Block is operating in Frame Generator/Frame Synchronizer Configuration # 23

If the DS3/E3 Framer block is configured to operate in Frame Generator/Frame Synchronizer Configuration # 23, then the Primary Frame Synchronizer block will be operating in the Egress Direction and the Secondary Frame Synchronizer block will be operating in the Ingress Direction, as depicted below in Figure 11-1.

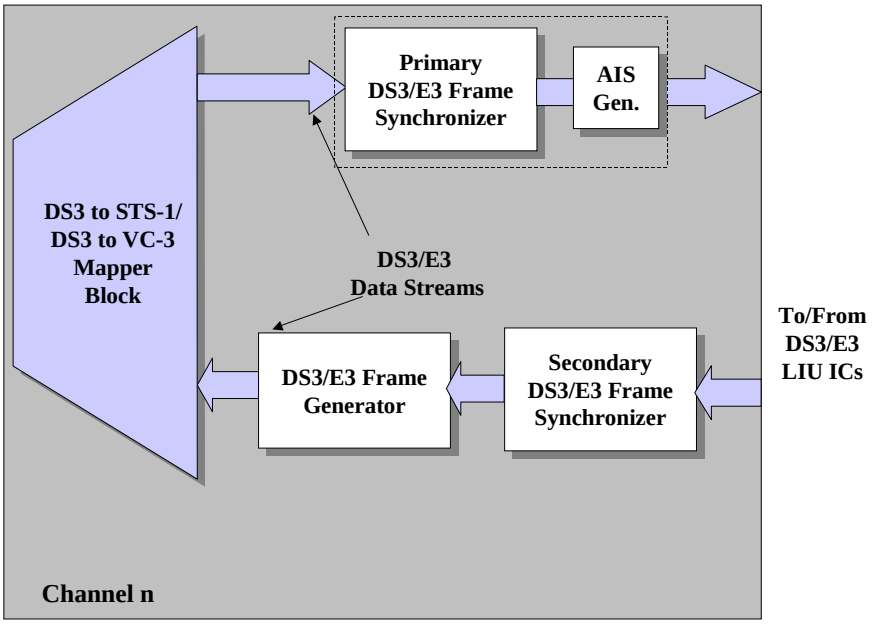

Figure 11-1, Illustration of Frame Generator/Frame Synchronizer Configuration # 23

Based upon this Frame Generator/Frame Synchronizer configuration, the user can configure the Channel to operate in the Single-Rail Mode by executing the following two steps.

STEP 1 – Set Bit 2 (Secondary Frame – Single Rail Input) within the "Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer" Register to "1" as depicted below.

Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer (Indirect Address = 0xNE, 0xF0; Direct Address = 0xNFF0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused			Primary Frame - Clock Output Invert	Primary Frame – Transmit AIS Enable	Secondary Frame – Single-Rail Input	Primary Frame - Dual-Rail Output	Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	1	0	0

This step configures the Secondary Frame Synchronizer block to operate in the Single-Rail Mode (e.g., to accept Single-Rail data from the DS3/E3 LIU IC, in the Ingress Direction).

STEP 2 – Set Bit 1 (Primary Frame – Dual-Rail Output) within the "Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer" register to "0" as depicted below.

Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer (Indirect Address = 0xNE, 0xF0; Direct Address = 0xNFF0)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused			Primary Frame - Clock Output Invert	Primary Frame – Transmit AIS Enable	Secondary Frame – Single-Rail Input	Primary Frame - Dual-Rail Output	Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	1	0	0

This step configures the Primary Frame Synchronizer block to operate in the Single-Rail Mode (e.g., outputs Single-Rail data to the DS3/E3 LIU IC, in the Egress Direction).

Once the user has executed these steps, then the DS3/E3 Framer block will be exchanging data with the DS3/E3 LIU IC in a Single-Rail Manner.

If the DS3/E3 Framer Block is operating in Frame Generator/Frame Synchronizer Configuration # 28

If the DS3/E3 Framer block is configured to operate in Frame Generator/Frame Synchronizer Configuration # 28, then the Primary Frame Synchronizer block will be operating in the Ingress Direction, and the DS3/E3 Frame Generator block will be operating in the Egress Direction, as depicted below in Figure 11-2.

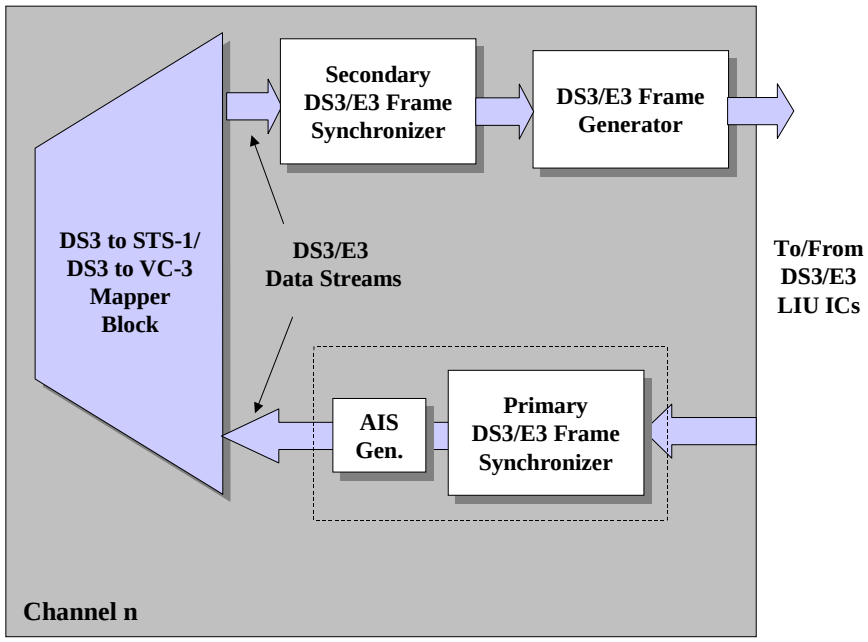

Figure 11-2, Illustration of Frame Generator/Frame Synchronizer Configuration # 28

Based upon this Frame Generator/Frame Synchronizer configuration, the user can configure the Channel to operate in the Single-Rail Mode, by executing the following step.

STEP 1 – Set Bit 3 (Single-Rail/Dual-Rail) within the "I/O Control" Register to "1" as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3/STS1 CLK OUT Invert	DS3/E3/ STS1 CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	0	0	0

This step configures the Primary Frame Synchronizer block to operate in the Single-Rail Mode (e.g., to accept Single-Rail data from the DS3/E3 LIU IC, in the Ingress Direction). Further, this step also configures the DS3/E3 Frame Generator block to operate in the Single-Rail Mode (e.g., to output Single-Rail data to the DS3/E3 LIU IC, in the Egress Direction).

Q11.2: Can the STS-1/STM-0 LIU Interface of the XRT94L43 device be configured to operate in the Dual-Rail Mode?

A11.2: No, the STS-1/STM-0 LIU Interfaces (within the XRT94L43 device) can only be configured to operate in the Single-Rail Mode.

Q11.3: Suppose that one wishes to operate the DS3/E3 Framer block in Frame Generator/Frame Synchronizer Configuration # 28, and if this user also wishes to interface four (4) XRT73L03 devices to the XRT94L43 device. What configuration steps should one do to make this work properly?

A11.3: The user should execute all of the following steps.

STEP 1 – The user must connect the LIU IC to the XRT94L43 device, in the manner as depicted below in Figure 11-3.

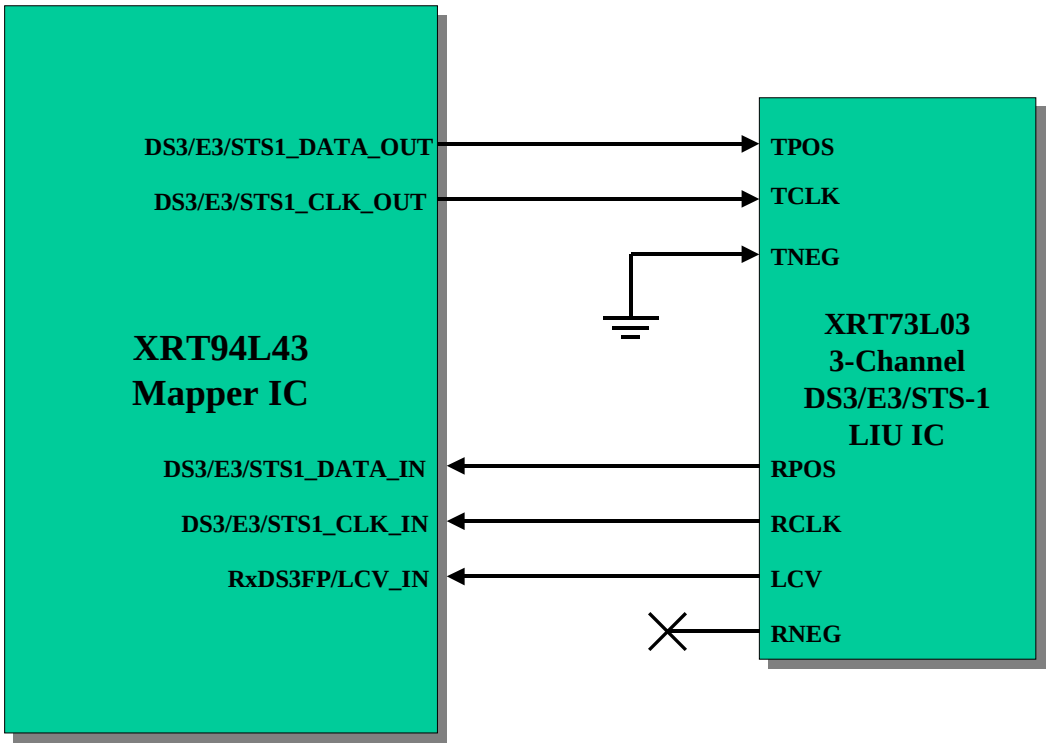

Figure 11-3, Simple Illustration of our recommendation on how to interface the XRT73L03 3-Channel DS3/E3/STS-1 LIU to the XRT94L43 Mapper Device

SOME NOTES ABOUT FIGURE 11-3:

a. The TNEG (TxNEG or TNDATA) input pins to the LIU IC must be tied to GND.
b. In the case of the XRT73L03/XRT73LC03 devices, the user should connect the dedicated "LCV" output pin to the "RxDS3FP/LCV" input pin of the XRT94L43 device. The RNEG output pin (from the LIU IC) can be left floating.

STEP 2 - Configure a given channel to operate in the DS3/E3 Mode.

This is accomplished by setting bits 1 (Receive – Ingress – STS-1 Enable) and 0 (Transmit – Egress – STS-1 Enable), within the "Mapper Control" Register, each to "0", as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control Register – Byte 2" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 3 – Configure the Jitter Attenuator Blocks to be able to support DS3/E3 Signals.

This can be accomplished by setting Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register – Byte 0" to "[0, X]" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	X	0	0	0	0	0

STEP 4 – Configure the DS3/E3 Framer Block to operate in Frame Generator/Frame Synchronizer Configuration # 28.
An illustration of "Frame Generator/Frame Synchronizer" Configuration # 28 is presented below in Figure 11-4.

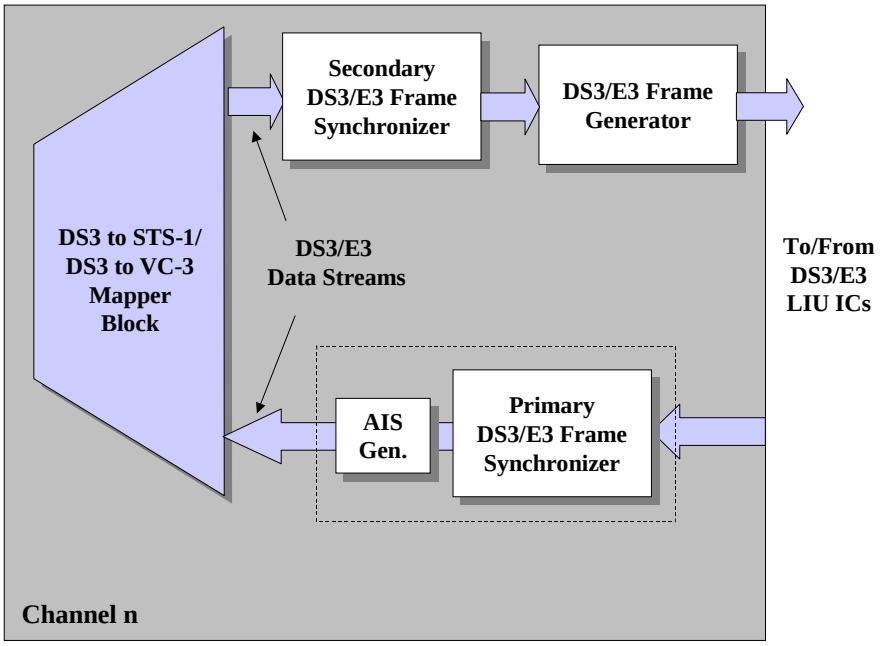

Figure 11-4, An Illustration of "Frame Generator/Frame Synchronizer" Configuration # 28

NOTE: The user can execute STEP 4, by writing the value "0xE6" into the "Mapper Control – T3/E3 Routing Register" as depicted below.

Mapper Control Register – T3/E3 Routing Register Byte (Indirect Address = 0xN6, 0x13; Direct Address = 0xN713)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	1	1	0

NOTE: The number "N" (which is used in the address location for the "Mapper Control" Register – T3/E3 Routing Register" ranges from 0x01 through 0x0C (for each of the 12 DS3/E3 Framer block channels within the XRT94L43 device).

STEP 5 – Configure the "DS3/E3 Framer" block to operate in the "desired" Data-Rate/Framing format.

This is accomplished by setting Bits 6 (IsDS3) and 2 (Frame Format) within the "Operating Mode Register" to the appropriate values, as presented below in Table 11-1. The bit-format of the "Operating Mode" Register, with these bit-fields "high-lighted" is also presented below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	X	1	0	1	X	1	1

Table 11-1, The Relationship between Bits 6 (IsDS3), Bit 2 (Frame Format) and the Corresponding Data-Rate/Frame Format of the DS3/E3 Framer Block

Bit 6 (IsDS3)	Bit 2 (Frame Format)	Resulting Framing Format
0	0	E3, ITU-T G.751
0	1	E3, ITU-T G.832
1	0	DS3, C-bit Parity
1	1	DS3, M13

STEP 6 – Configure the Frame Generator block to operate in the "Local-Timing/Frame Slave" Mode.

This is accomplished by setting the TimRefSel[1:0] bit-fields, within the Operating Mode Register to "[0, 1]", as depicted below.

Operating Mode Register (Indirect Address = 0xNE, 0x00; Direct Address = 0xNF00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Interrupt Enable RESET	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	X	1	0	1	X	0	1

This step configures the Frame Generator block to generate the outbound DS3/E3 Frames, based upon some "Frame Alignment" information being provided to it by the "up-stream" Frame Synchronizer block (which is typically the Secondary Frame Synchronizer block).

STEP 7 – Configure the Primary Frame Synchronizer block to accept data (from the LIU IC) in a Single-Rail Manner, and configure the Frame Generator Block to output data (to the LIU IC) in a Single-Rail Manner.

Both of these configuration settings can be achieved by setting Bit 3 (Single-Rail/Dual-Rail), within the "I/O Control Register", to "1", as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3/STS1 CLK OUT Invert	DS3/E3/ STS1 CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	0	0	0

STEP 8 – Configure the XRT94L43 device to output the Egress DS3/E3 data on the appropriate Egress Direction clock edge, and to sample the Ingress DS3/E3 data, on the appropriate Ingress Direction clock edge, such that XRT94L43 and LIU set-up and hold time requirements are not violated.

We will first address our clock-edges/timing in the Egress Direction. Afterwards, we will address our clock-edges/timing in the Ingress Direction.

Addressing Clock Edges/Timing in the Egress Direction

In the Egress Direction, we need to decide which edge of the "Egress Direction" clock (from the XRT94L43 device) that we need to clock out our DS3/E3 data, towards the LIU IC. Prior to implementing these configuration settings, a little timing analysis is "in-order".

XRT94L43 Clock to Output Delay Characteristics for DS3/E3 Applications

In the Egress Direction, the XRT94L43 device will output the "Egress Direction" DS3/E3 data upon either the rising of falling edges of the "Egress Direction" clock signal. These output signals will be routed to the "Transmit Digital" Clock and Data Inputs of the XRT73L03 device. The "Clock-to-Output" delay capability of the XRT94L43 device is as presented below in both Figure 11-5 and Table 11-2.

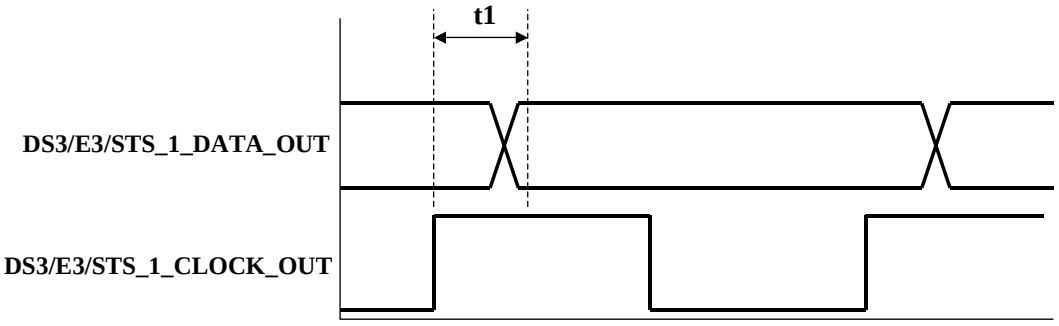

Figure 11-5, Illustration of the Timing Waveform for the Egress Output of the XRT94L43 device (Please see Table 11-2 for value of t1)

NOTE: As mentioned earlier, the XRT94L43 device can be configured to output the "DS3/E3/STS-1_DATA_OUT" signal upon either the rising or falling edge of "DS3/E3/STS-1_CLOCK_OUT". Figure 11-5 presents an illustration of the Timing Wave-form (with these signal) with the "DS3/E3/STS-1_DATA_OUT" being updated upon the rising edge of "DS3/E3/STS-1_CLOCK_OUT".

Table 11-2, Egress Direction Clock to Output Delays for the XRT94L43 Device (DS3/E3 Applications)

Symbol	Description	Min.	Typ.	Max.
t1	Rising Edge of "DS3/E3/STS-1_CLOCK_OUT" to "DS3/E3/STS-1_DATA_OUT" output delay	0ns		4ns

LIU Set-up and Hold Time Requirements in the Egress Direction

In the Egress Direction, the LIU IC has the responsibility of sampling the "outbound" DS3/E3 data that is being applied to its "TPDATA" input pin, upon either the rising or falling edge of the TCLK input pin. By default, the XRT73L03 device will be configured to sample the "TPDATA" input pin upon the falling edge of TCLK. The set-up and hold time requirements for the LIU IC are as presented below in both Figure 11-6 and Table 11-3.

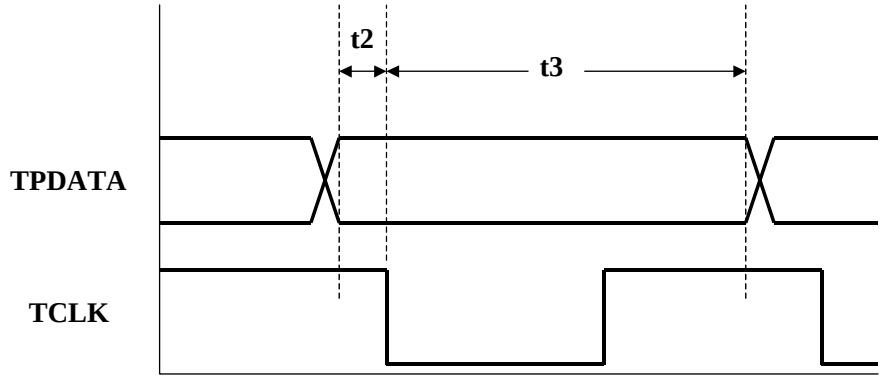

Figure 11-5, Illustration of the Timing Waveform for the Transmit Input of the XRT73L03 LIU IC (Please see Table 11-2 for values of t2 and t3)

Table 11-3, Set-up and Hold Time Requirements for the XRT73L03 device

Symbol	Description	Min.	Typ.	Max.
t2	TPDATA to falling edge of TCLK set-up time requirements	3ns		
t3	Falling edge of TCLK to TPDATA Hold time requirements	3ns		

Analysis of the Egress Direction Timing Information

If the XRT94L43 device is configured to output its Egress Direction data upon the rising edge of the Egress Direction clock signal, and if the LIU IC is configured to sample this Egress Direction data upon the falling edge of the Egress Direction clock signal, then the resulting set-up and hold times (for each of the Data Rates) is as presented below, for each of the two data-rates.

Table 11-4, Results of Egress Direction Timing Analysis – DS3/E3 Applications

Data Rate	Current Situation		LIU Requirements	
	Minimum Set-up Time	Minimum Hold Time	Set-up Time	Hold Time
E3	11.5ns	14.5ns	3ns	3ns
DS3	7.2ns	11.2ns	3ns	3ns

The analysis of this Egress Direction Timing Information indicates that there will be NO timing problems if all of the following is true.

a. The XRT94L43 device is configured to output the Egress Direction DS3/E3 data upon the rising edge of the Egress Direction clock, and
b. The XRT73L03 LIU IC is configured to sample the Egress Direction DS3/E3 data upon the falling edge of the Egress Direction clock signal.

Implementing this configuration within the XRT94L43 device (for the Egress Direction)

If the user has selected Frame Generator/Frame Synchronizer Configuration # 28, then the user can configure the XRT94L43 device to output the Egress Direction DS3/E3 data upon the rising edge of the Egress Direction Clock signal by setting Bit 2 (DS3/E3 CLKOUT Invert), within the "I/O Control Register" to "0", as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3 CLK OUT Invert	DS3/E3/ CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	0	0	0

NOTE: Each Channel, within the XRT73L03 LIU IC will (by default) be configured to sample the "Egress" Data upon the falling edge of the "Egress Direction" clock signal.

Addressing Clock Edges/Timing in the Ingress Direction

In the Ingress Direction, we need to decide which edge of the "Ingress Direction" clock (from the LIU IC) that the XRT94L43 must use to sample to Ingress Direction DS3/E3 data. Prior to implementing these configuration settings, a little timing analysis is "in-order".

XRT73L03 Clock to Output Delay Characteristics

In the Ingress Direction, the XRT73L03 device will output the "Ingress Direction" DS3/E3/STS-1 data upon either the rising or falling edges of the "Ingress Direction" (or LIU Recovered) clock signal. These output signals will be routed to the "Ingress" Inputs of the XRT94L43 device. The "Clock-to-Output" delay capability of the XRT73L03 device is as presented below in both Figure 11-7 and Table 11-5.

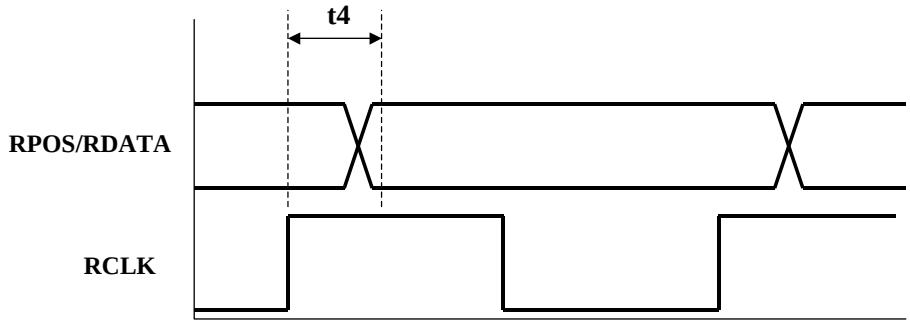

Figure 11-7, Illustration of the Timing Waveform for the Receive (Ingress Direction) Output of the XRT73L03 device (Please see Table 11-5 for value of t4)

Table 11-5, Receive (Ingress) Direction Clock to Output Delays for the XRT73L03 Device

Symbol	Description	Min.	Typ.	Max.
t4	Rising Edge of "RCLK" to "RPOS/RDATA" output delay	0ns	2.5ns	4ns

XRT94L43 Set-up and Hold Requirements in the Ingress Direction

In the Ingress Direction, the XRT94L43 IC has the responsibility of sampling the "inbound" DS3/E3 data that is being applied to its "DS3/E3/STS-1_DATA_IN" input pin, upon either the rising or falling edge of "DS3/E3/STS-1_CLOCK_IN" input pin. The set-up and hold time requirements for the XRT94L43 IC are as presented below in both Figure 11-8 and Table 11-6.

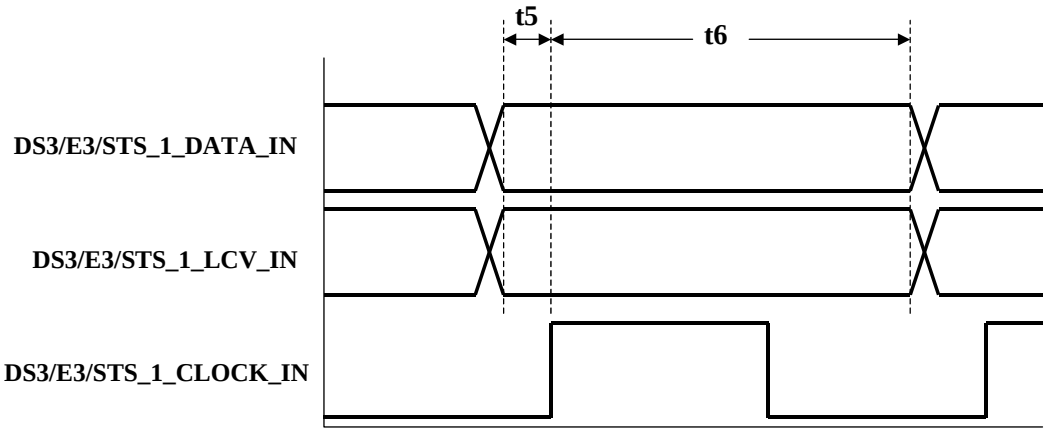

Figure 11-8, Illustration of the Timing Waveform for the Ingress Input of the XRT94L43 Mapper IC (Please see Table 11-6 for values of t5 and t6)

Table 11-6, Set-up and Hold Time Requirements for the XRT94L43 Mapper IC (For DS3/E3 Applications Only)

Symbol	Description	Min.	Typ.	Max.
t5	DS3/E3/STS-1_DATA_IN and DS3/E3/STS-1_LCV_IN" to rising edge of DS3/E3/STS-1_CLOCK_IN" set-up time requirements	7ns		
t6	Rising edge of DS3/E3/STS-1_CLOCK_IN to DS3/E3/STS-1_DATA_IN and DS3/E3/STS-1_LCV_IN" Hold time requirements	0ns		

Analysis of the Ingress Direction Timing Information

If the XRT73L03 device is configured to output its Recovered Data upon the rising edge of the Ingress Direction (or Recovered) Clock signal, and if the XRT94L43 device is configured to sample this Ingress Direction data upon the rising edge of the Ingress Direction clock signal, then the resulting set-up and hold-times (for each of the Data Rates) is as presented below in Table 11-7.

Table 11-7, Results of Ingress Direction Timing Analysis (for DS3/E3 Applications)

Data Rate	Current Situation		XRT94L43 Requirements	
	Minimum Set-up Time	Minimum Hold Time	Set-up Time	Hold Time
E3	25.1ns	0ns	7ns	0ns
DS3	18.3ns	0ns	7ns	0ns

The analysis of this Ingress Direction Timing Information indicates that there will be NO timing problems if all of the following is true.

a. The XRT73L03 device is configured to output the Ingress Direction DS3/E3 data upon the rising edge of the Ingress Direction (e.g., Recovered) Clock signal, and
b. The XRT94L43 device is configured to sample the Ingress Direction DS3/E3/STS-1 data upon the rising edge of the Ingress Direction clock signal.

Implementing this configuration with the XRT94L43 devices (for the Ingress Direction)

If the user has selected Frame Generator/Frame Synchronizer Configuration # 28, then the user can configure the XRT94L43 device to sample the Ingress Direction DS3/E3 data upon the rising edge of the Ingress Direction Clock signal by setting Bit 1 (DS3/E3 CLK IN Invert) to "1" as depicted below.

I/O Control Register (Indirect Address = 0xNE, 0x01; Direct Address = 0xNF01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ Zero-Sup*	Single-Rail/ Dual-Rail	DS3/E3 CLK OUT Invert	DS3/E3/ CLK IN Invert	Reframe
R/W	R/O	R/W	R/W	R/O	R/W	R/W	R/W
1	0	1	0	1	0	1	0

Q11.4: Suppose that one wishes to interface four (4) XRT73L03 devices to the XRT94L43 device, and to support the transmission of STS-1/STM-0 data. What configuration steps should one do to make this work properly?

A11.4: The user should execute all of the following steps.

STEP 1 – The user must connect the LIU IC to the XRT94L43 device, in the manner as depicted below in Figure 11-9.

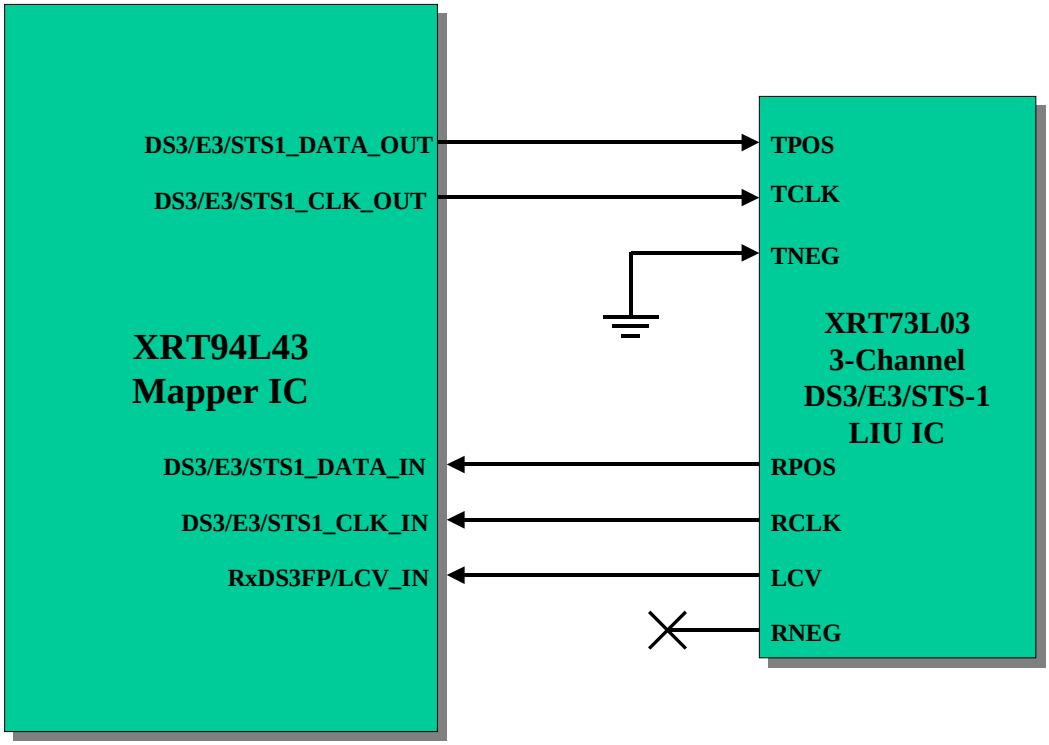

Figure 11-9, Simple Illustration of our recommendation on how to interface the XRT73L03 3-Channel DS3/E3/STS-1 LIU to the XRT94L43 Mapper Device

SOME NOTES ABOUT FIGURE 11-9:

a. The TNEG (TxNEG or TNDATA) input pins to the LIU IC must be tied to GND.
b. In the case of the XRT73L03/XRT73LC03 device, the user should connect the dedicated "LCV" output pin to the "RxDS3FP/LCV" input pin of the XRT94L43 device. The RNEG output pin (from the LIU IC) can be left floating.

STEP 2 – Configure a given channel to operate in the STS-1 Mode

This is accomplished by setting bits 1 (Receive – Ingress – STS-1 Enable) and 0 (Transmit – Egress – STS-1 Enable), within the "Mapper Control" Register, each to "1" as depicted below.

Mapper Control Register – Byte 2 (Indirect Address = 0xN6, 0x01; Direct Address = 0xN701)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

NOTE: The number "N" (which is used in the address location for the "Mapper Control Register – Byte 2" ranges from 0x01 through 0x0C (for each of the 12 STS-1 block channels within the XRT94L43 device).

STEP 3 – Configure the Jitter Attenuator Blocks to be able to support STS-1 Signals

This can be accomplished by setting Bits 6 and 5 (SDH JA Freq_Sel[1:0]) within the "Mode Control Register – Byte 0" to "[1, 1]" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
APS Recovery Time Mode Disable	SDH JA Freq_Sel[1:0]		Unused	AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	1	1	0	0	0	0	0

STEP 4 – Configure the XRT94L43 device to output the Egress (or Transmit) STS-1 data on the appropriate Egress Direction clock edge, and to sample the Ingress (or Receive) STS-1 data, on the appropriate Ingress Direction clock edge, such that XRT94L43 and LIU set-up and hold time requirements are not violated.

We will first address our clock-edges/timing in the Egress (Transmit) Direction. Afterwards, we will address our clock-edges/timing in the Ingress (Receive) Direction.

Addressing Clock Edges/Timing in the Egress (Transmit) Direction

In the Egress Direction, we need to decide which edge of the "Egress Direction" clock (from the XRT94L43 device) that we need to clock out our STS-1 data, towards the LIU IC. Prior to implementing these configuration settings, a little timing analysis is "in-order".

XRT94L43 Clock to Output Delay Characteristics for STS-1 Applications

In the Egress Direction, the XRT94L43 device will output the "Egress Direction" STS-1 data upon either the rising or falling edges of the "Egress Direction" clock signal. These output signals will be routed to the "Transmit Digital" Clock and Data Inputs of the XRT73L03 device. The "Clock-to-Output" delay capabilities of the XRT94L43 device is as presented below in both Figure 11-10 and Table 11-8.

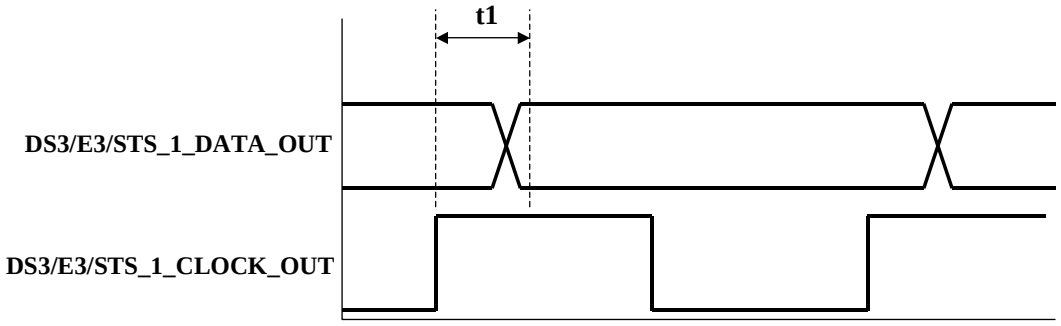

Figure 11-10, Illustration of the Timing Waveform for the Egress Output of the XRT94L43 device (Please see Table 11-8 for value of t1)

NOTE: As mentioned earlier, the XRT94L43 device can be configured to output the "DS3/E3/STS-1_DATA_OUT" signal upon either the rising or falling edge of "DS3/E3/STS-1_CLOCK_OUT". Figure 11-10 presents an illustration of the Timing Wave-form (with these signals) with the "DS3/E3/STS-1_DATA_OUT" signal being updated upon the rising edge of "DS3/E3/STS-1_CLOCK_OUT".

Table 11-8, Egress Direction Clock to Output Delays for the XRT94L43 Device (STS-1 Applications)

Symbol	Description	Min.	Typ.	Max.
t1	Rising Edge of "DS3/E3/STS-1_CLOCK_OUT" to "DS3/E3/STS-1_DATA_OUT" output delay	0ns		3ns

LIU Set-up and Hold Time Requirements in the Egress Direction

In the Egress (Transmit) Direction, the LIU IC has the responsibility of sampling the "outbound" STS-1 data that is being applied to its "TPDATA" input pin, upon either the rising or falling edge of the TCLK input pin. By default, the XRT73L03 device will be configured to sample the "TPDATA" input pin upon the falling edge of TCLK. The set-up and hold time requirements for the LIU IC are as presented below in both Figures 11-11 and Table 11-9.

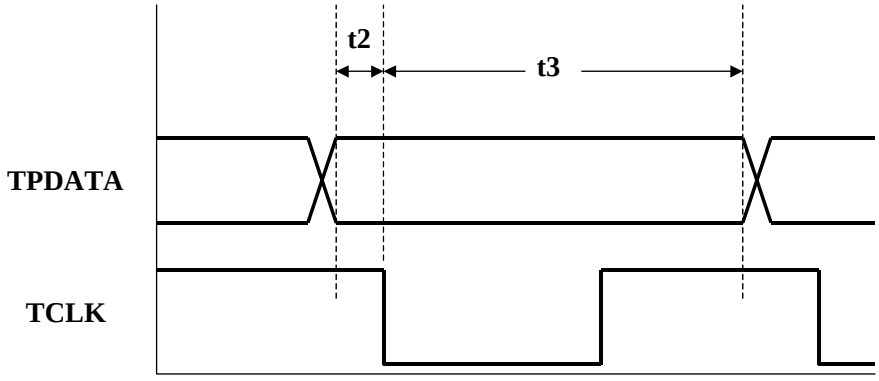

Figure 11-11, Illustration of the Timing Waveform for the Transmit Input of the XRT73L03 LIU IC (Please see Table 11-9 for values of t2 and t3)

Table 11-9, Set-up and Hold Time Requirements for the XRT73L03 device

Symbol	Description	Min.	Typ.	Max.
t2	TPDATA to falling edge of TCLK set-up time requirements	3ns		
t3	Falling edge of TCLK to TPDATA Hold time requirements	3ns		

Analysis of the Egress (Transmit) Direction Timing Information
If the XRT94L43 device is configured to output its Egress (or Transmit) Direction data upon the rising edge of the Egress Direction clock signal, and if the LIU IC is configured to sample this Egress Direction data upon the falling edge of the Egress Direction clock signal, then the resulting set-up and hold times is as presented below, for STS-1 applications.

Table 11-10, Results of Egress Direction Timing Analysis – STS-1 Applications

Data Rate	Current Situation		LIU Requirements	
	Minimum Set-up Time	Minimum Hold Time	Set-up Time	Hold Time
STS-1	6.6ns	9.6ns	3ns	3ns

The analysis of this Egress Direction Timing information indicates that there will be NO timing problems if all of the following is true.

The XRT94L43 device is configured to output the Egress Direction STS-1 upon the rising edge of the Egress Direction clock, and

The XRT73L03 LIU IC is configured to sample the Egress Direction STS-1 data upon the falling edge of the Egress Direction clock signal.

Implementing this configuration within the XRT94L43 device (for the Egress Direction)

The user can configure the XRT94L43 device to output the Egress Direction STS-1 data upon the rising edge of the Egress Direction Clock signal by setting Bit 2 (Transmit STS-1 Clock Invert), within the "Mapper Control Register – Byte 1" to "0" as depicted below.

Mapper Control Register – Byte 1 (Indirect Address = 0xN6, 0x02; Direct Address = 0xN702)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 FIFO SW RESET	Unused			Receive STS-1 Clock Invert	Transmit STS-1 Clock Invert	DEFAULT R	DEFAULT O
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: Each Channel, within the XRT73L03 LIU IC will (by default) be configured to sample the "Egress" Data upon the falling edge of the "Egress Direction" clock signal.

Addressing Clock Edges/Timing in the Ingress (Receive) Direction

In the Ingress Direction, we need to decide which edge of the "Ingress (or Receive) Direction" clock (from the LIU IC) that the XRT94L43 device must use to sample the Ingress Direction STS-1 data. Prior to implementing these configuration settings, a little timing analysis is "in-order".

XRT73L03 Clock to Output Delay Characteristics

In the Ingress Direction, the XRT73L03 device will output the "Ingress Direction" DS3/E3/STS-1 data upon either the rising or falling edges of the "Ingress Direction" (or LIU Recovered) clock signal. These output signals will be routed to the "Ingress" Inputs of the XRT94L43 device. The "Clock-to-Output" delay capability of the XRT73L03 device is as presented below in both Figure 11-12 and Table 11-11.

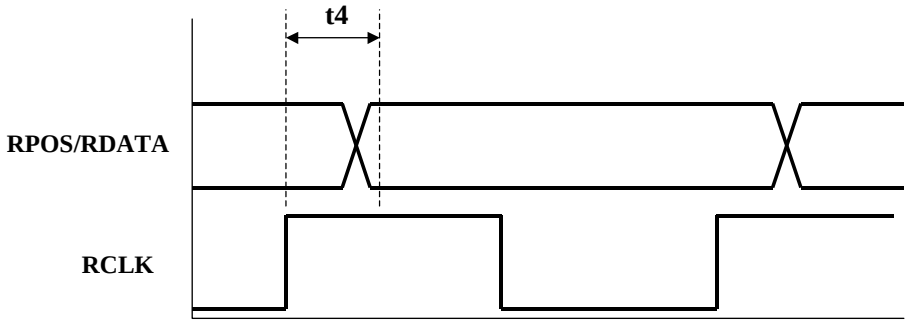

Figure 11-12, Illustration of the Timing Waveform for the Receive (Ingress Direction) Output of the XRT73L03 device (Please see Table 11-11 for value of t4)

Table 11-11, Receive (Ingress) Direction Clock to Output Delays for the XRT73L03 Device

Symbol	Description	Min.	Typ.	Max.
t4	Rising Edge of "RCLK" to "RPOS/RDATA" output delay	0ns	2.5ns	4ns

XRT94L43 Set-up and Hold Time Requirements in the Ingress Direction

In the Ingress Direction, the XRT94L43 IC has the responsibility of sampling the "inbound" STS-1 data that is being applied to its "DS3/E3/STS-1_DATA_IN" input pin, upon either the rising or falling edge of "DS3/E3/STS-1_CLOCK_IN" input pin. The set-up and hold time requirements for the XRT94L43 IC are as presented below in both Figures 11-13 and Table 11-12.

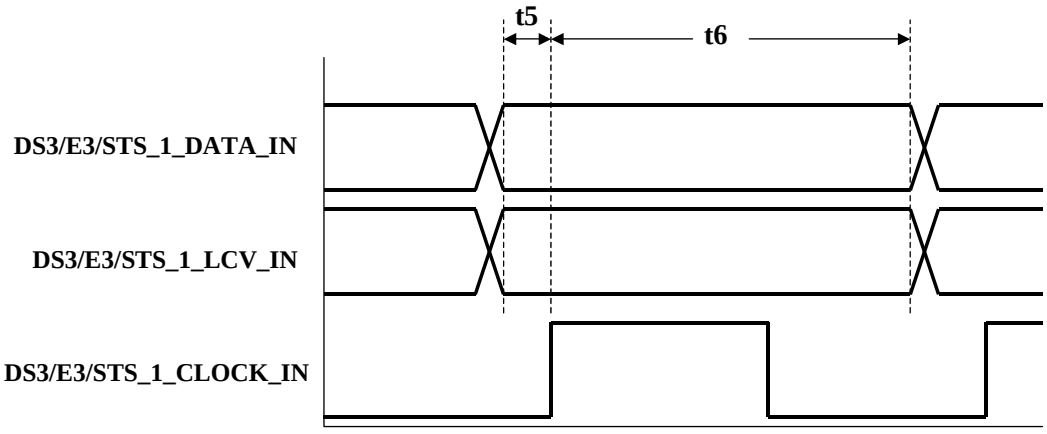

Figure 11-13, Illustration of the Timing Waveform for the Ingress Input of the XRT94L43 Mapper IC (Please see Table 11-6 for values of t5 and t6)

Table 11-12, Set-up and Hold Time Requirements for the XRT94L43 Mapper IC (For STS-1 Applications Only)

Symbol	Description	Min.	Typ.	Max.
t5	DS3/E3/STS-1_DATA_IN and DS3/E3/STS-1_LCV_IN" to rising edge of DS3/E3/STS-1_CLOCK_IN" set-up time requirements	4ns		
t6	Rising edge of DS3/E3/STS-1_CLOCK_IN to DS3/E3/STS-1_DATA_IN and DS3/E3/STS-1_LCV_IN" Hold time requirements	0ns		

Analysis of the Ingress Direction Timing Information

If the XRT73L03 device is configured to output its Recovered Data upon the rising edge of the Ingress Direction (or Recovered) Clock signal, and if the XRT94L43 device is configured to sample this Ingress Direction data upon the rising edge of the Ingress Direction clock signal, then the resulting set-up and hold-times (for STS-1 applications) is as presented below in Table 11-13.

Table 11-13, Results of Ingress Direction Timing Analysis (for STS-1 Applications)

Data Rate	Current Situation		XRT94L43 Requirements	
	Minimum Set-up Time	Minimum Hold Time	Set-up Time	Hold Time
STS-1	15.3ns	0ns	4ns	0ns

The analysis of this Ingress Direction Timing Information indicates that there will be NO timing problems if all of the following is true.

a. The XRT73L03 device is configured to output the Ingress Direction STS-1 data upon the rising edge of the Ingress Direction (e.g., Recovered) Clock signal, and
b. The XRT94L43 device is configured to sample the Ingress Direction STS-1 data upon the rising edge of the Ingress Direction clock signal.

Implementing this configuration with the XRT94L43 devices (for the Ingress Direction)

The user can configure the XRT94L43 device to sample the Ingress Direction STS-1 data upon the rising edge of the Ingress Direction Clock signal by setting Bit 3 (Receive STS-1 Clock Invert) to "0" as depicted below.

Mapper Control Register – Byte 1 (Indirect Address = 0xN6, 0x02; Direct Address = 0xN702)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-1 FIFO SW RESET	Unused			Receive STS-1 Clock Invert	Transmit STS-1 Clock Invert	DEFAULT R	DEFAULT O
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Q12: SDH Related Questions

Q12.1: Can the XRT94L43 device be configured to support both SDH/AU-3 and SDH/TUG-3 Mapping?

A12.1: The answer to this question is "Yes, the XRT94L43 device can be configured to support either SDH Mapping Mode. In fact, in the case of the XRT94L43 device, it is possible to configure portions of the device to operate in the SDH/AU-3 Mapping Mode, and the remaining portions operating in the SDH/TUG-3 Mapping Mode. The procedure for configuring the XRT94L43 device into either one of these modes is presented below.

Configuring the XRT94L43 device to operate in the SDH/AU-3 Mapping Mode
The user can configure the XRT94L43 device to operate in the SDH/AU-3 Mapping Mode by executing the following two steps.

STEP 1 – Set Bit 3 (SDH/SONET*), within the Receive STS-12 Transport Control Register – Byte 0" to "1" as depicted below.

Receive STS-12 Transport Control Register – Byte 0 (Indirect Address = 0x04, 0x03; Direct Address = 0x0503)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-N OH Extract	SF Detect Enable	SD Detect Enable	Descramble Disable	SDH/ SONET*	REI-L Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

This step configures the XRT94L43 device to operate in the SDH Mode.

STEP 2 – Set Bits 3 through 0 (AU3-n/TUG-n*), within the "Mode Control Register – Byte 0" to "1" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	1	1	1	1

This step configures the entire XRT94L43 device to operate in the SDH/AU-3 Mapping Mode.

Once the user has executed these three steps, then the XRT94L43 device will now be configured to operate in the “Functional Block Diagram” as presented below in Figure 12-1.

Frequently Asked Questions regarding the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/STM-4 Mapper IC

Preliminary

August 15, 2006

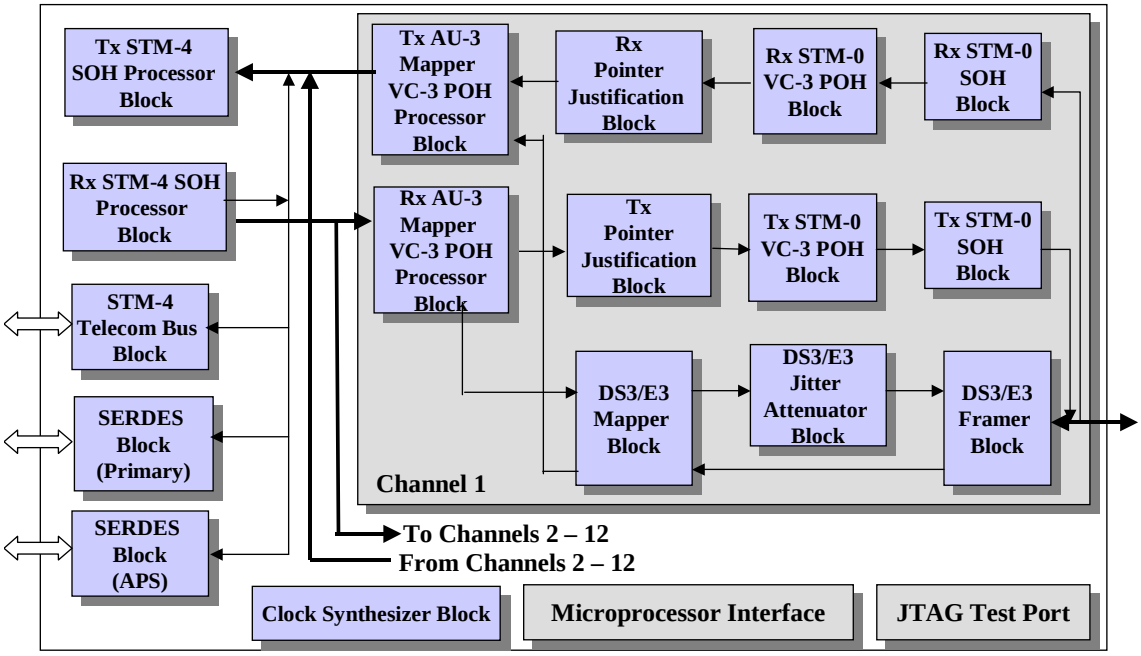

Figure 12-1, Functional Block Diagram of the XRT94L43 Device, when it has been configured to operate in the SDH/AUG-3 Mapping Mode

Configuring the XRT94L43 device to operate in the SDH/TUG-3 Mapping Mode
The user can configure the XRT94L43 device to operate in the SDH/TUG-3 Mapping Mode by executing the following two steps.

STEP 1 – Set Bit 3 (SDH/SONET*), within the Receive STS-12 Transport Control Register – Byte 0" to "1" as depicted below.

Receive STS-12 Transport Control Register – Byte 0 (Indirect Address = 0x04, 0x03; Direct Address = 0x0503)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STS-N OH Extract	SF Detect Enable	SD Detect Enable	Descramble Disable	SDH/ SONET*	REI-L Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

This step configures the XRT94L43 device to operate in the SDH Mode.

STEP 2 – Set Bits 3 through 0 (AU3-n/TUG-n), within the "Mode Control Register – Byte 0" to "0" as depicted below.

Mode Control Register – Byte 0 (Indirect Address = 0x00, 0x1B; Direct Address = 0x011B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused				AU3_3/ TUG_3*	AU3_2/ TUG_2*	AU3_1/ TUG_1*	AU3_0/ TUG_0*
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

This step configures the entire XRT94L43 device to operate in the SDH/TUG-3 Mapping Mode.

Once the user has executed these three steps, then the XRT94L43 device will now be configured to operate in the "Functional Block Diagram" as presented below in Figure 12-2.

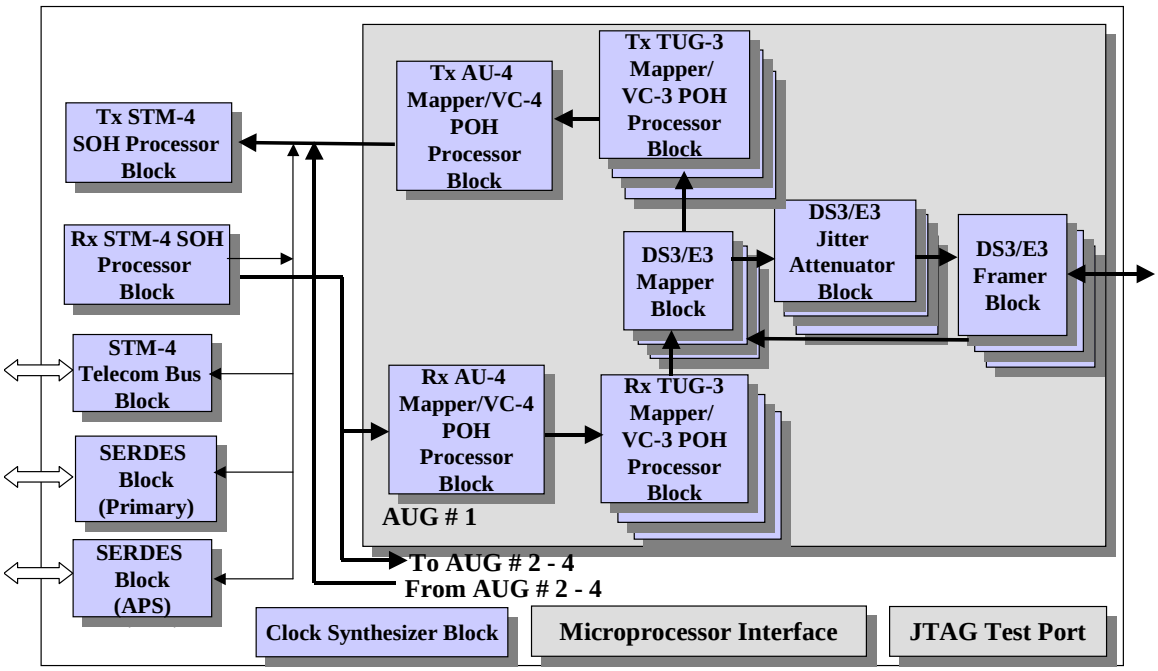

Figure 12-2, Functional Block Diagram of the XRT94L43 Device, when it has been configured to operate in the SDH/TUG-3 Mapping Mode

Q12.2: If the XRT94L43 device has been configured to operate in the SDH/TUG-3 Mapping Mode, is there a way to read out the contents of the VC-4 POH bytes, within the incoming STM-4 data-stream via the Microprocessor Interface?

A12.2: Yes, the user can always obtain the value of the most recently received VC-4 POH bytes by reading out the contents of the following nine (9) or 36 registers.

Receive AU-4 Mapper/VC-4 Path – Receive J1 Byte Capture Register
(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xD3; Direct Address = 0xD1D3)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xD3; Direct Address = 0xD9D3)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xD3; Direct Address = 0xE1D3)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xD3; Direct Address = 0xE9D3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This particular register contains the value for the J1 byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive B3 Byte Capture Register
(AU-4 Mapper/VC-4 Channel 0 – Indirect Address = 0xD0, 0xD7; Direct Address = 0xD1D7)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xD7; Direct Address = 0xD9D7)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xD7; Direct Address = 0xE1D7)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xD7; Direct Address = 0xE9D7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This particular register contains the value for the B3 byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive C2 Byte Capture Register

(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xDB; Direct Address = 0xD1DB)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xDB; Direct Address = 0xD9DB)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xDB; Direct Address = 0xE1DB)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xDB; Direct Address = 0xE9DB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This register contains the value of the C2 byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive G1 Byte Capture Register

(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xDF; Direct Address = 0xD1DF)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xDF; Direct Address = 0xD9DF)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xDF; Direct Address = 0xE1DF)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xDF; Direct Address = 0xE9DF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This register contains the value of the G1 byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive F2 Byte Capture Register

(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xE3; Direct Address =0xD1E3)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xE3; Direct Address = 0xD9E3)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xE3; Direct Address = 0xE1E3)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xE3; Direct Address = 0xE9E3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This register contains the value of the F2 byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive H4 Byte Capture Register

(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xE7; Direct Address =0xD1E7)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xE7; Direct Address = 0xD9E7)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xE7; Direct Address = 0xE1E7)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xE7; Direct Address = 0xE9E7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This register contains the value of the H4 byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive Z3 Byte Capture Register

(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xEB; Direct Address =0xD1EB)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xEB; Direct Address = 0xD9EB)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xEB; Direct Address = 0xE1EB)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xEB; Direct Address = 0xE9EB)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This register contains the value of the Z3 byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive Z4 (K3) Byte Capture Register

(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xEF; Direct Address = 0xD1EF)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xEF; Direct Address = 0xD9EF)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xEF; Direct Address = 0xE1EF)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xEF; Direct Address = 0xE9EF)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This register contains the value of the Z4 (K3) byte, within the most recently received VC-4 frame.

Receive AU-4 Mapper/VC-4 Path – Receive Z5 Byte Capture Register
(AU-4 Mapper/VC-4 Channel 0 - Indirect Address = 0xD0, 0xF3; Direct Address = 0xD1F3)
(AU-4 Mapper/VC-4 Channel 1 – Indirect Address = 0xD8, 0xF3; Direct Address = 0xD9F3)
(AU-4 Mapper/VC-4 Channel 2 – Indirect Address = 0xE0, 0xF3; Direct Address = 0xE1F3)
(AU-4 Mapper/VC-4 Channel 3 – Indirect Address = 0xE8, 0xF3; Direct Address = 0xE9F3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

This register contains the value of the Z5 byte, within the most recently received VC-4 frame.

Q13: Transmit and Receive STS-12 TOH Processor Block Related Questions

Q13.1: Does the XRT94L43 device permit the user to control the values of certain TOH bytes, within the outbound STS-12 signal, via on-chip registers?

A13.1: Yes, the circuitry associated with the Transmit STS-12 TOH Processor block (within the XRT94L43 device) permits the user control all of the following TOH bytes, via on-chip register.

- K1
- K2
- M1
- S1
- F1
- E1
- E2
- J0

The on-chip registers associated with each of these TOH bytes are presented below.

For the K1 Byte:

Transmit STS-12 Transport – K1K2 (APS) Value Register – Byte 0 (Indirect Address = 0x08, 0x2F; Direct Address = 0x092F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_K1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the K2 Byte:

Transmit STS-12 Transport – K1K2 (APS) Value Register – Byte 1 (Indirect Address = 0x08, 0x2E; Direct Address = 0x092E)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_K2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the M1 Byte:

Transmit STS-12 Transport – M0M1 Byte Value Register (Indirect Address = 0x08, 0x37; Direct Address = 0x0937)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_M0M1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the S1 Byte:

Transmit STS-12 Transport – S1 Byte Value Register (Indirect Address = 0x08, 0x3B; Direct Address = 0x093B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_S1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the F1 Byte:

Transmit STS-12 Transport – F1 Byte Value Register (Indirect Address = 0x08, 0x3F; Direct Address = 0x093F)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_F1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the E1 Byte:

Transmit STS-12 Transport – E1 Byte Value Register (Indirect Address = 0x08, 0x43; Direct Address = 0x0943)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_E1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the E2 Byte:

Transmit STS-12 Transport – E2 Byte Value Register (Indirect Address = 0x08, 0x47; Direct Address =0x0947)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_E2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

For the J0 Byte:

Transmit STS-12 Transport – Transmit J0 Byte Value Register (Indirect Address = 0x08, 0x4B; Direct Address = 0x094B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit_J0_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NOTE: The Transmit STS-12 Transport – J0 Byte Value Register should only be used if the user selected a "Section Trace" Message" size of 1 byte.

Q13.2: Does the XRT94L43 device permit the user to monitor the values of certain TOH bytes by software (via on-chip registers) within the inbound STS-12 signal, via on-chip registers?

A13.2: Yes, in fact the XRT94L43 device permits the user to have access to ALL TOH bytes within the incoming STS-12 signal (that has been received via the Receive STS-12 TOH Processor block) via the "Receive TOH Capture Buffer".

Q13.3: Can the user configure the Transmit STS-12/STM-4 PECL Interface block to align its transmit of an STS-12 or STM-4 frame, with an external 8kHz signal?

A13.3: The answer to this question is "Yes". The Transmit STS-12/STM-4 PECL Interface block can be configured to align its transmission of outbound STS-12/STM-4 frames with an 8kHz pulse that is applied to the "TxSBFP" input pin.

Ordinarily, the Transmit STS-12/STM-4 PECL Interface block will align its transmission of STS-12/STM-4 frames such that it will transmit the very first bit of a given STS-12/STM-4 frame during the same "77.76MHz clock" period that the "TxSBFP" input pin is "pulsed" high. However, if desired, the user can configure the Transmit STS-12/STM-4 PECL Interface block to transmit the very first bit of an "outbound" STS-12/STM-4 frame, a few "77.76MHz clock" periods AFTER "TxSBFP" has been pulsed "high".

This can be achieved by writing the appropriate value into the "STS-12/STM-4 Telecom Bus Control Register – Byte 3 and Byte 2" as depicted below.

STS-12/STM-4 Telecom Bus Control Register – Byte 3 (Indirect Address = 0x00, 0x34; Direct Address = 0x0134)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HRSYNC_Delay[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

STS-12/STM-4 Telecom Bus Control Register – Byte 2 (Indirect Address = 0x00, 0x35; Direct Address = 0x0135)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HRSYNC_Delay[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

These two registers present a "16-bit" Latency Register. The "STS-12/STM-4 Telecom Bus Control Register – Byte 3" is the "Upper Byte" Register, and the "STS-12/STM-4 Telecom Bus Control Register – Byte 2" is the "Lower Byte" Register.

If the user writes the value "0x0001" into this register, then the Transmit STS-12/STM-4 PECL Interface block will be configured to transmit the very first byte of a given "outbound" STS-12/STM-4 frame, one "77.76MHz clock" period, after the "TxSBFP" input pin has been pulsed "high" by the 8kHz signal. If the user writes the value "0x0002" into this register, then the Transmit STS-12/STM-4 PECL Interface block will be configured to transmit the very first byte of a given "outbound" STS-12/STM-4 frame,

two “77.76MHz clock” periods after the “TxSBFP” input pin has been pulsed “high” by the 8kHz signal, and so on.